

**HP 3000 SERIES II  
COMPUTER SYSTEM  
MANUAL OF STAND-ALONE DIAGNOSTICS**

**STAND-ALONE HP 30031A  
SYSTEM CLOCK/CONSOLE DIAGNOSTIC**

Diagnostic No. D425A



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## I. INTRODUCTION

The Stand-Alone HP 30031A System Clock/Console Interface Test verifies the functional level operation of the Console Interface and the System/Clock card. The diagnostic is capable of diagnosing the problems related to bit misconfiguration of the counting-register, limit-register and counting rate selector-register. Additionally, the interrupts and overflow conditions are tested as well as CIO (Control I/O) command bits and status bits associated with the system Clock/Console interface.

## II. MINI-OPERATING INSTRUCTIONS

### A. Operations

1. Cold Load Diag File# (Associated with D425A) from non-CPU Cold Load Tape.
2. Respond to Speed-Sense by asserting "CR" at the console.
3. Respond to dialogue at the Console.

### B. Switch-Register Options

<u>Bit#</u>	<u>Function</u>
0	Select External Switch Register
1	Set To change Section Switch Register
2	Set To Bypass Operator Intervention (Section 5) :Steps 506, 510, 512, 514, 520)
3	Spare
4	Spare
5	Loop Current Section
6	Spare
7	Output To Line Printer (if configured in SDUP)
8	Spare
9	Suppress Non-Error Messages
10	Suppress Error Messages
11	Loop On Last Step
12	Halt On Error
13	Halt At The End Of Step
14	Halt At The End Of Section
15	Halt After A Complete Program Cycle

## II.

### C. Section Switch-Register Options

<u>Bit#</u>	<u>Function</u>
0	Re-Configure
1	Select Section 1
2	Select Section 2
3	Select Section 3
4	Select Section 4
5	Select Section 5 (Select only when console is connected to the Clock/Console Interface PCA.)
6-15	Spare

### D. Halt Assignments

<u>No. (octal)</u>	<u>Function</u>
0	Halt For Switch Entry (Ext. Reg.)
1	Halt For Switch Entry (Section Select)
2	Halt For Switch Entry (Restore Ext. Reg.)
3	Halt On Error Count Reached
4-6	Spare
7	Halt For Step 506 Key Entry
10	Halt For Step 510 Key Entry
11	Halt For Steps 510, 520 Key Entry
12	Halt For Error
13	Halt After Step
14	Halt After Section
15	Halt After Complete Program Cycle
16	Halt For Steps 512
17	Halt For Step 514 Key Entry

## III. REQUIREMENTS

### A. Hardware

The hardware required to run the system Clock/Console interface diagnostic is the minimum HP 3000 Series II computer system.

B. Software

The Stand-Alone Diagnostic Utility Program (SDUP) is required to create the Stand-Alone Diagnostic tape. The tape is comprised of Cold Load program, the Relocating Loader, and one or more diagnostic programs including the Stand-Alone HP 30031A System Clock/Console Interface Test; ALL the programs are coded in System Programming Language (SPL).

IV. DETAILED OPERATING INSTRUCTIONS

A. Operating Instructions

The following are the instructions for loading, executing, and configuring the Stand-Alone HP 30031A System Clock Console Interface Test:

1. Cold Load by entering %3006 into the Switch-Register and simultaneously depress "LOAD" and "ENABLE" switches on the CPU Front Panel.
2. Select an appropriate Diagnostic File # (associated with the System Clock/Console Diagnostic) and enter the number into the Switch-Register. Depress "RUN" switch. The diagnostic tape supplied is identified by file names and their respective file position on the tape. The selected program is now loaded into memory. The tape rewinds at the end of program load.
3. The Diagnostic program is now executable.
4. Depress "RETURN" key on the console to respond to the Speed-Sense. Then the program prints the diagnostic header information and requests necessary parameters to begin the diagnostic cycle.

## B. Options

Under Stand-Alone HP 30031A System Clock/Console Interface Test, the operator can control the test sections to be executed; control halts after sections or steps or upon program completion; control suppression of error and non-error messages; and control loop on a specific test step. These control options may be entered when the program requests for a specific option entry via the test dialogue.

It should be noted, however, that the test program has been pre-configured to be executable in its best load and go configuration.

1. The following describes the options associated with each bit of the Switch-Register for a program request of an option entry for the message type:

### Q02 SELECT SWREG OPTIONS

<u>Bit#</u>	<u>Function</u>
0	Select External Switch Register
1	Set to change Section Selection Register
2	Set to bypass operator intervention (Section 5)
3	Spare
4	Spare
5	Loop current Section
6	Spare
7	Output to Line Printer (if configured in SDUP)
8	Spare
9	Suppress non-error messages
10	Suppress error messages
11	Loop on last step
12	Halt on error
13	Halt at end of Section
14	Halt at end of Section
15	Halt after a complete program cycle

If both bits (0 and 1) are either (00) or (01) then the previously configured values are used for the execution. In the case for an initial state, the pre-defined values (best load and go conditions) for both "Switch Register Options" and "Section Switch Register Options" are used.



1. (Continued)

If bits (0 and 1) are (10) then only the Switch Register content is changed. The Section Switch Register content will not be altered and the previously configured Section Switch Register Options are used for the execution.

If both bits (0 and 1) are (11) then the contents of both "SWITCH REGISTER" and the "SECTION SWITCH REGISTER" are altered after an appropriate option entry.

2. The following describes the options associated with each bit of the Section Select Switch Register for the program request for a following message type:

Q03 SELECT SECTION SWREG OPTIONS

Section Switch Register Options

<u>Bit#</u>	<u>Function</u>
0	Re-configure
1	Select Section 1
2	Select Section 2
3	Select Section 3
4	Select Section 4
5	Select Section 5 (Select only when connected to the Clock/Console Interface PCA)
6-15	Spare

Some test steps in Section 5 require an operator intervention.

These steps are:

- . Step 506 (Test Break Key Status Bit 12)
- . Step 510 (Echoplex ON/OFF test)
- . Step 512 (Input Data Overrun test)
- . Step 514 (Input Data Ready test)
- . Step 520 (No Reset test)

## C. Halts and message tables

### 1. Halt Assignments

When a program halts, a code is displayed in the Current Instruction Register (CIR). This is displayed as (0 011 000 011 11X XXX: where X's is the halt #).

#### Halt Code Assignments

<u>Bits 12-15 (CIR)</u>	<u>Assignments</u>
0	Halt for Switch Register Entry (Ext.)
1	Halt for Switch Register Entry (Section Select)
2	Halt for Switch Register Entry (Restore Ext.)
3	Halt on error count reached
4-6	Spare
7	Step 506: Press Run then momentarily press BREAK Key on the console device.
10	Step 510: Echoplex On test: Press Run, enter any number of characters followed by a Carriage Return, and observe that characters are echoed.
11	Step 510: Echoplex Off test: Press Run, enter any number of characters followed by a Carriage Return, and observe that characters are not echoed. Step 520: Depress any key several times and press Run.
12	Halt for error
13	Halt after step
14	Halt after Section
15	Halt after a complete program cycle
16	Step 512: Input data overrun test: Rapidly and repeatedly depress any characters on the console device, then press Run.
17	Step 514: Depress the BREAK Key several times and press Run.

## 2. Message Formats

There are four types of message classifications:  
D,E,P, and Q classes.

### D-class

Messages which describe program boundaries. Some operator intervention is required.

### E-class

Messages related to error numbers. Some operator intervention is required.

### P-class

Messages which describe the test completion of a section or a step. Some operator intervention is required.

### Q-class

Messages which a program request some parameter entry be made. Operator intervention is required.

## 2.1 Actual Message Descriptor

### 2.1.1 D01 30031A SYSTEM TIMER DIAGNOSTIC (D425X.YY.ZZ)

:Header information for this diagnostic program; where

X = Version number

YY = Update number

ZZ = Fix number

### 2.1.2 D02 END: PROGRAM CYCLE: PASS = XXXXXX

:This message indicates number of test passes the program has completed for those test sections selected.

### 2.1.3 D03 HALT: COMPLETE PROGRAM CYCLE

:This message is yield whenever bit #15 of the SWREG OPTION is recognized as being "On".

### 2.1.4 Q01 ENTER SYSTEM TIMER DEVICE # =

:Program request for an appropriate console/timer device # entry.

- 2.1.5 Q02 SELECT SWREG OPTIONS  
:Program is requesting any of the option entry available and described in Section B.1.
- 2.1.6 Q03 SELECT SECITON SWREG OPTIONS  
:Program is requesting any of the option entry available and described in Section B.2.
- 2.1.7 Q04 ENTER MAXIMUM ERROR COUNT #=  
:Program is requesting a maximum number of error count as an entry. The maximum count which may be entered is 9999.
- 2.1.8 Q05 RESTORE SWREG OPTIONS  
(Same option entry as those requested in Section C.2.1.5)
- 2.1.9 P01 SECTION XX  
:This message indicates the Section number which will be in execution.
- 2.1.10 P02 END SECTION XX  
:This message indicates the Section number which has just been completed.
- 2.1.11 P04 END STEP XXX  
:This message indicates that the test step in execution was just completed.
- 2.1.12 P05 HALT: STEP XXX  
:This message indicates that the computer is in a halt state after completing the indicated step.
- 2.1.13 P06 HALT: SECTION XX  
:This message indicates that the program is in a halt state after completing the indicated section.

2.1.4 P08 ERROR: HALT STEP XXX

:This message indicates an error occurrence within the test step specified.

2.1.15 P09 MAX. ERROR COUNT REACHED.

:This message indicates that the error count which has been either entered or pre-defined has been reached. The computer will be in a halt state.

2.1.16 Exxx

:This message indicates the appropriate error number associated with the actual error.

2.1.17 STATUS=X XXX XXX XXX XXX XXX

:This message displays the actual data appropriate to the test.

2.1.18 SHOULD=X XXX XXX XXX XXX XXX

:This message displays the expected value.

D. Pre-Configuration Options

1. The diagnostic program has been preconfigured to execute in best load and go configuration using the options available from Sections IV.B.1 and IV.B.2. The pre-configured values can be altered when the diagnostic cold load tape is being created under SDUP (System Diagnostic Utility Program).

2. The following are the DB Locations containing data that can be changed during pre-configuration using SDUP:

- DB+0 Switch Register Setting
- DB+1 Section Register Setting
- DB+2 Version and Update Level
- DB+3 30031A DRT Number
- DB+4 Maximum Error Print Count

E. Control and Status word Formats

1. Control Word Format.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	B	C	D	E			F	G	H	I	J	K	L	M	
A															

(A) Master Clear. To function as Master Clear, bit #3 of this word must be a Logic 0.

E.

1. Control Word (Continued)
- B CR Count Rate. These three bits determine the count rate for the CR (when Bit #3 is a Logic 1). Count rate selection is available from Count Rate Selection Table.
- Ⓒ Master clear/count rate selection. A Logic 1 in this bit field designates that bits 0-2 will be used as the selection of the counting rate for the CR. A Logic 0 enables bit #0 (see A above) to function as master clear. When this bit is Logic 0 then bits 1 and 2 are not used.
- Ⓓ Enables Interface Interrupts. A Logic 1 enables interrupt requests from the serial interface function of the system clock/serial interface PCA to reach the CPU (providing the group interrupt mask is enabled).
- Ⓔ Selective Interrupt Clear. These three bits selectively clear each process which generates an interrupt request. See Selective Interrupt Clear Table which shows the bit patterns necessary to selectively clear each interrupt process.
- Ⓕ Reset CR after LR=CR interrupt. A Logic 1 in this bit-field causes the CR to be reset after an interrupt request is generated by LR=CR process.
- Ⓖ LR/CR Function Selection. A Logic 0 in this bit-field causes R10 and W10 commands to address Limit Register (LR), if control word bit #12 is a Logic 1. A Logic 1 in this bit-field causes R10 and W10 commands to address the Counting Register (CR), if control word bit #12 is a Logic 1.
- Ⓗ Clear All Interrupts. A Logic 1 in this bit-field clears all logic on the subsystem PCA which generates an interrupt request to the CPU.
- Ⓘ Enable Echoplex. A Logic 1 enables the echoplex function on the system clock/serial Interface PCA. The echoplex functions when enabled, routes serial data received from the external device back to the external device for outputting.
- Ⓙ Interface/Clock Selection. A Logic 0 in this bit-field routes R10 and W10 commands to the serial interface function on the System Clock/Serial Interface PCA. A Logic 1 routes R10 and W10 commands to the System Clock Function on the System Clock/Serial Interface PCA.
- Ⓚ Function unassigned.

E.

1. (Continued)

- L Reset Interface. A Logic 1 in this bit-field initializes the serial interface logic on the system Clock/Serial Interface PCA.
- M Enable Clock Interrupts. A Logic 0 in this bit-field inhibits interrupt requests from the system clock logic from reaching the CPU. A Logic 1 enables interrupt requests from the system clock logic to reach the CPU (providing the group interrupt mask for the subsystem is enabled).

1.1 Counting Rate Selection Table.

Control Word Bits			Count Rate
0	1	2	
0	0	0	1 Microseconds
0	0	1	10 Microseconds
0	1	0	100 Microseconds
0	1	1	1 Millisecond
1	0	0	10 Milliseconds
1	0	1	100 Milliseconds
1	1	0	1 Second
1	1	1	10 Seconds

1.2 Selective Interrupt Clear Table

Control Word Bits			Interrupt Process Cleared
5	6	7	
0	0	0	No clearing
0	0	1	LR=CR
0	1	0	LR=CR overflow
0	1	1	I/O System Interrupt (SIN)
1	0	0	Data Overrun
1	0	1	Input Data Ready
1	1	0	Ready to output
1	1	1	Received CR Error

2. Status Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	B	C		D	E	F	G	H	I	J	K	L	M	N	

- Ⓐ SIO OK. This bit is permanently at Logic 0. A Logic 0 indicates that the subsystem is incapable of operating in SIO mode.
- Ⓑ RIO, WIO OK. This bit is permanently at Logic 1. A Logic 1 indicates that the subsystem PCA is capable of executing RIO and WIO commands.
- Ⓒ CR Count Rate. These three bits reflect the count rate of the CR the Count Rate was determined by bits 0-2 of the control word from the Counting Rate Selection Table.
- Ⓓ Data Overrun. A Logic 1 indicates a character has transferred from the external device to the subsystem PCA before the preceding character from the external device has transferred from the subsystem PCA to the CPU. Thus, causing the second character to overlay the first character in a register on the subsystem PCA, and the first character is lost. An interrupt request is also generated when the Data Overrun bit becomes a Logic 1.
- Ⓔ Input Data Ready. A Logic 1 indicates that the subsystem PCA has received a character or a break signal from the external device. Once set, the bit remains a Logic 1 until a RIO command transfers the character to the CPU, or until the input data ready Logic is cleared. An interrupt request is generated when Input Data Ready becomes a Logic 1.
- Ⓕ Ready to Output. A Logic 1 indicates that the subsystem PCA is ready to accept a WIO command and a character from the CPU. This bit becomes a Logic 0 when WIO command is received, and remains a Logic 0 until the character is serially transferred to the external device. An interrupt request is generated when ready to output becomes a Logic 1.



2. Status Word Format (Continued)

- Ⓔ Data Terminal Ready. A Logic 1 indicates that the external device is ready to transmit or receive data. This bit reflects the state of the Data Terminal Ready signal from the external device.
- Ⓕ Read CR Error. A Logic 1 indicates that a RIO command was issued to read the content of the CR when the CR was incrementing. Thus, the count obtained from the CR is invalid.
- Ⓖ LR=CR. A Logic 1 indicates that the count placed in the LR has been reached by the CR. An interrupt request is generated when the LR=CR bit becomes a Logic 1.
- Ⓙ LR=CR Overflow. A Logic 1 indicates that the CR has reached the count in the LR two times without being serviced by an interrupt. An interrupt request is generated when the LR=CR overflow bit becomes a Logic 1.
- Ⓚ Break Received. A Logic 1 indicates that the subsystem PCA has received a break signal from the external device. This bit remains a Logic 1 until the break signal is terminated by a stop bit. To prevent multi interrupt requests from the Subsystem PCA (Input Data Ready and Data Overrun), all interrupts from the interface function of the subsystem PCA must be disabled (Control Word Bit #4) when the Break Received Interrupt is detected.
- Ⓛ I/O System Interrupt. A Logic 1 indicates that the Subsystem PCA has received a Set Interrupt (SIN) command from the CPU. An interrupt request is generated when this bit becomes a Logic 1.
- Ⓜ LR/CR Selection Status. A Logic 0 indicates that a RIO or a WIO commands address the LR (if the Control Word Bit #12 is a Logic 1). A Logic 1 indicates that a RIO or a WIO commands address the CR (if Control Word Bit #12 is a Logic 1).
- Ⓝ Control Word Bit #8 Selection Status. A Logic 1 indicates that the CR is reset after an interrupt request is generated by the LR=CR signal.

V. Detailed Test Description

Stand-alone HP 30031A System Clock/Console Interface Test comprises six test sections and the test description for each test step within each of the six test sections is given below:

1. Section 1

This section tests Counting Register and Limit Register with loaded data patterns to verify the integrity of each bit of the registers. Also tested are interrupts and overflows conditions.

1.1 Step 101

Tests setting the Counting and the Limit Registers using all possible 8 bit patterns. The CRS is set to time base of 1 millisecond. Initially; CR=0, and LR=CR+1. Then both LR and CR are incremented progressively with a TIO in a loop until CR=377.

1.1.1 Step 101 Error Codes and messages

E101

STATUS = 0 000 000 OXX XXX XXX

SHOULD = 0 000 000 000 000 000

Ignore "SHOULD" message. The "STATUS" contains the LR counter value when the time out counter expired for LR ≠ CR.

E707

STATUS = 0 000 000 001 000 001

SHOULD = 0 000 000 OXX XXX XXX

The "STATUS" contains the step number for this test. The "SHOL" contains the device number for the non-responding device.

E102

STATUS = 0 000 000 0XX XXX XXX

SHOULD = 0 000 000 0YY YYY YYY

The "STATUS" contains the CR counter value and the "SHOULD" contains the LR counter value when the compare (LR and CR) error occurred.

1.2 Step 103

Tests CR=LR interrupt with 1 millisecond time base. Initially, LR=1, CR=0.

1.2.1 Step 103 Error Codes and Messages

E103

STATUS = 0 000 000 000 000 000

SHOULD = 0 000 000 000 000 000

Ignore both "STATUS" and "SHOULD" contents. The error code "103" indicates that an interrupt for LR = CR was not generated within the time allotted.

E104

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 100 001

"STATUS" contains the device status.

"SHOULD" contains the expected status.

This error message is generated when LR=CR interrupt is not noted in device status.

E707 (Same error as in step 101)

E106

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 000 000 000 000 000

The "STATUS" contains the content of CR. The "SHOULD" contains the expected CR content.

1.3 Step 105

Tests for overflow when CR>LR. The test uses 100 microsecond time base. Waits approximately 700 microseconds for the overflow to occur.

1.3.1 Step 105 Error Codes and Messages

E105

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 110 001

The "STATUS" contains the actual device status when sampled after time allotted is expired. The "SHOULD" contains the expected status.

2. Section 2

This section tests for CR=LR for all allowed counting rates.

2.1 Table

Steps	Increment	CRS (Binary)	CR (Octal)	LR (Octal)	Time Interval
Step 201	1 μsec	000	000000	000144	100 μsec
Step 202	10 μsec	001	000000	000012	100 μsec
Step 203	100 μsec	010	000000	000004	400 μsec
Step 204	1 msec	011	000000	000004	4 msec
Step 205	10 msec	100	000000	000004	40 msec
Step 206	100 msec	101	000000	000004	400 msec
Step 207	1 sec	110	000000	000004	4 sec
Step 210	10 sec	111	000000	000004	40 sec

2.2 Steps 201-210 Error Codes and messages. All the errors messages within this section occur when LR≠CR within the time allotted.

2.2.1 Step 201

E201

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 000 100 100 000

2.2.2 Step 202

E202

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 100 100 100 000

2.2.3 Step 203

E203

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 100 000

2.2.4 Step 204

E204

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 100 000

2.2.5 Step 205

E205

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 110 000 100 100 000

2.2.6 Step 206

E206

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 110 100 100 100 000

2.2.7 Step 207

E207

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 000 100 100 000

2.2.8 Step 210

E210

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 100 100 100 000

3. Section 3

This section tests CIO command bits associated with the System Clock.

3.1 Step 302

This test validates CIO command bits 5-7 (001) which resets LR=CR interrupt.

3.1.1 Step 302 Error Message

E302

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 000 000

This message is given when bit 10 of the status word becomes a Logic 1 after a LR=CR condition and is not a logic 0 when reset LR=CR interrupt command is issued.

3.2 Step 304

This test validates the CIO command bits 5-7 (010) which resets CR>LR overflow.

### 3.2.1 Step 304 Error Messages

E304

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 000 000

This message is given when bit 11 of the status word becomes a Logic 1 after a CR>LR condition is forced and is not a Logic 0 when reset CR>LR overflow interrupt command is issued.

### 3.3 Step 306

This test validates the CIO command bits 5-7 (011) which resets the interrupt generated by a Set Interrupt (SIN) instruction.

#### 3.3.1 Step 306 Error Messages

E306

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 110 100

This message is given when SIN instruction is executed and bit 13 of the status is not reflected to a Logic 1.

E307

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 110 000

This message is given when reset SIN interrupt command is issued and the bit 13 of the status word is not reflected to a Logic 0.

### 3.4 Step 310

This test validates the master reset command clears interrupts

#### 3.4.1 Step 310 Error Messages

E310

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 000 000

This message is given when LR=CR and CR>LR overflow interrupts are forced and the Master Reset command is issued to reset those interrupts. Status word bits 10-11 should reflect the change from a Logic 1 to a Logic 0.

### 3.5 Step 312

This test validates the Master Reset for the entire board.

### 3.5.1 Step 312 Error Messages.

E312

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 000 000

Test condition not set up. Just one-shot Master Reset command is issued.

### 3.6 Step 314

Using CIO command bit 8, the test resets CR after each interrupt.

#### 3.6.1 Step 314 Error Messages

E314

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 000 000 000 000 000

This message is given when the content of the CR is not equal to 0 after reset LR=CR interrupt command is issued. Ignore this message if "STATUS" contains the device status.

### 3.7 Step 316

This test validates the clock interrupt mask bit 15.

#### 3.7.1 Step 316 Error Messages

E316

STATUS = 0 000 000 000 000 000

SHOULD = 0 000 000 000 000 000

Ignore both "STATUS" and the "SHOULD" messages. The error code indicates that the LR=CR interrupt did not occur within the time allotted after enabling the clock interrupt (CIO bit 15).

## 4. Section 4

This section tests various status bits associated with the CIO commands for the system clock.

### 4.1 Step 402

This test validates status word bit 0 being always equal to 0 (SIO not allowed).

#### 4.1.1 Step 402 Error Messages

E402

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 100 000

This message is implied when at any time during 1000(10) TIO loops a status error occurs (bit 0≠0).

This test validates status word bit 1 being always equal to 1 (RIO/WIO allowed).

#### 4.2.1 Step 404 Error Message

E404

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 100 000

This message is implied when at any time during 1000 (10) TIO loops a status error occurs (bit 1  $\neq$  1).

#### 4.3 Step 406

This test validates setting bits 2-4 of the status word to 000 by issuing CIO command bits 0-2 with 000.

##### 4.3.1 Step 406

E406

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 000 100 000 001

#### 4.4 Step 407

This test validates setting bits 2-4 of the status word to 001 by issuing CIO command bits 0-2 with 001.

##### 4.4.1 Step 407 Error Message

E407

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 100 100 000 001

#### 4.5 Step 410

This test validates setting bits 2-4 of the status word to 010 by issuing CIO command bits 0-2 with 010.

##### 4.5.1 Step 410 Error Message

E410

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 000 001

#### 4.6 Step 411

This test validates setting bits 2-4 of the status word to 011 by issuing CIO command bits 0-2 with 011.

##### 4.6.1 Step 411 Error Message

E411

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 000 001



#### 4.7 Step 412

This test validates setting bits 2-4 of the status word to 100 by issuing CIO command bits 0-2 with 100.

##### 4.7.1 Step 412 Error Message

E412

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 110 000 100 000 001

#### 4.8 Step 413

This test validates setting bits 2-4 of the status word to 101 by issuing CIO command bits 0-2 with 101.

##### 4.8.1 Step 413 Error Messages

E413

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 110 100 100 000 001

#### 4.9 Step 414

This step validates setting bits 2-4 of the status word to 110 by issuing CIO command bits 0-2 with 110.

##### 4.9.1 Step 414 Error Message

E414

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 000 100 000 001

#### 4.10 Step 415

This step validates setting bits 2-4 of the status word to 111 by issuing CIO command bits 0-2 with 111.

##### 4.10.1 Step 415 Error Message

E415

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 100 100 000 001

#### 4.11 Step 420

This step validates bit 9 (Read CR Error) of the status word by causing the Read CR Error condition (bit 9 to a Logic 1) within the time allocated. Then CIO command bits 5-7 (111) is issued to reset bit 9 of the status word to a Logic 0.

#### 4.11.1 Step 420 Error Message

E707

STATUS = 0 000 000 100 010 000

SHOULD = 0 000 000 0XX XXX XXX

This message is implied when CCL (non-responding device ) exist after issuing a RIO command to the clock device. The "STATUS" contains the step number of the error occurrence and the "SHOULD" contains the device number.

E420

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 000 101 000 010

This message is implied when bit 9 (Read CR Error) of the status word does not become a Logic 1 within the time allocated.

E421

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 100 000 100 110 000

This message is implied when a CIO command is issued to reset Read CR Error but bit 9 (Read CR Error) of the status word does not become a Logic 0.

#### 4.12 Step 422

This step validates bit 15 of the status word by causing a LR=CR condition and then issuing CIO command to reset CR after LR>CR interrupt which reflects bit 15 of the status word to become a Logic 1.

#### 4.12.1 Step 422 Error Message

E422

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 000 100 000 011

This message is implied when CIO command to reset CR after LR=CR interrupt is issued but bit 15 of the status word is not reflected (does not become a Logic 1).

#### 4.13 Step 424

This test validates bit 14 of the status word equal to "0" when bits 9 and 12 (command word) are equal to "01".

4.13.1 Step 424 Error Message

E424

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 000 000

This message is implied when a LR=CR condition is forced and then CIO command to access LR is issued but after issuing TIO command to sense the device status bit 14 (Status Word) it is not a logic 0.

4.14 Step 426

This step validates bit 14 (Status Word) equal to "1" when bits 9 and 12 (command word) are "11".

4.14.1 Step 426 Error Message

E426

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 101 100 100 000 010

This message is implied when a LR=CR condition is forced and then CIO command to access CR is issued but after issuing TIO command to sense the device status bit 14 (status word) it is not a Logic 1.

5. Section 5

This section should be selected only when the console is connected to the Clock/Console Board.

This section tests CIO command bits and status bits associated with the Clock/Console interface. Some of the test steps in Section 5 require an operator intervention.

5.1 Step 502

This step enables the interface interrupts and sends a character and at the end of character transmission an interrupt should occur within the time allocated.

5.1.1 Step 502 Error Message

E502

STATUS = 0 000 000 000 000 000

SHOULD = 0 000 000 000 000 000

This message is implied when the interface does not interrupt within the allocated time.

- 5.2 Step 504  
 This test validates bit 14 (master reset to the console interface) which reflects bits 5,6 and 12 (Status Word) to become a Logic 1.
- 5.2.1 Step 504 Error Message  
 E504  
 STATUS = X XXX XXX XXX XXX XXX  
 SHOULD = 0 101 100 110 000 000  
 This message is implied when bits 5, 6 and 12 (status word) do not become a Logic 1.
- 5.3 Step 506  
 This test validates the Break Key Status bit 12. A HALT 7 occurs the operator should press "RUN" and depress the Break Key momentarily. The program waits approximately 60 seconds for the Break Key depression before an error is implied.
- 5.3.1 Step 506 Error Message  
 E506  
 STATUS = X XXX XXX XXX XXX XXX  
 SHOULD = 0 111 001 110 001 000  
 This message is implied when 60 second allocated time is expired.
- 5.4 Step 510  
 This test validates Echoplex ON and OFF. The program turns Echoplex ON and issues a Halt 10. Press "RUN" and type any number of characters on the console device terminated by a "Carriage Return". Observe Echoplex ON. Next, the Echoplex is turned OFF and HALT 11 is issued. Press "RUN" and type any number of characters on the console device terminated by a "Carriage Return". Observe Echoplex OFF.
- 5.4.1 Step 510 Error Message  
 (No error messages applicable)
- 5.5 Step 512  
 This test validates status bit 5 which indicates Data Overrun. A Halt 16 is issued. Rapidly depress any keys several times and press "RUN".

### 5.5.1 Step 512 Error Message

E512

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 011 110 100 001

This message is implied when after issuing a TIO command the bit 5 (Status Word) is not reflected to a Logic 1.

E513

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 011 110 100 001

This message is implied when bit 5 (Status Word) becomes a Logic 1 and then CIO command bits 5-7 (100) is issued to reset the Data Overrun but bit 5 (Status Word) is not reflected to a Logic 0.

### 5.6 Step 514

This test validates status bit 6 which indicates Input Data Ready. A HALT 17 is issued. Depress "Break" Key several times and then press "RUN".

#### 5.6.1 Step 514 Error Message

E514

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 011 110 101 000

This message is implied when after issuing a TIO command the status bit 6 is not reflected to a Logic 1.

E515

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 010 110 101 000

This message is implied when status bit 6 becomes a Logic 1 and then CIO command bits 5-7 (101) is issued to reset the Input Data Ready interrupt but status bit 6 is not reflected to a Logic 0

### 5.7 Step 516

This test validates status bit 7 which indicates Ready to Output. A character is transmitted and the TIO in a loop senses for a status bit 7 change to a Logic 1. If the change does not occur within the time allocated then the error is implied.

5.7.1 Step 516 Error Message

E516

STATUS = X XXX XXX XXX XXX XXX

SHOULD = 0 111 000 110 110 000

5.8 Step 520

This test validates CIO command bits 5-7 (000) which will function as no Reset Interrupt. A HALT 11 is issued. Depress any key several times and press "RUN".

5.8.1 Step 520 Error Message

E520

STATUS = X XXX XXX XXX XXX XXX

SHOULD = Y YYY YYY YYY YYY YYY

The "SHOULD" contains the status before the CIO command bits 5-7 (000) is issued. The "STATUS" contains the status after the CIO command 5-7 (000) is issued.