HP 3000 SERIES II/III
COMPUTER SYSTEMS
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE HP 30030B/C
SELECTOR CHANNEL DIAGNOSTIC

Diagnostic No. D429A

30030-90011
Printed in U.S.A.

7/78

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I. INTRODUCTION

The Stand-Alone HP-30030B/C Selector Channel Diagnostic program is designed to test the HP-30030B/C Selector Channel. The test is divided into sections with the first section performing a cursory check of the HP-30033A Selector Channel Maintenance Board (SCMB) by bypassing the Selector Channel with Direct I/O commands (executed via the I/O Processor and the IOP bus).

Each subsequent section communicates with the Maintenace Card via the Selector Channel and its associated Port Controller. These sections check data pattern response, control sequences, and I/O program orders. The sections are designed such that each succeeding section tests as little new hardware as possible until all data paths have been verified. In addition, the program is constructed so as to be multiplexer compatible, where possible, to facilitate maintenance on the SCMB.

Operator/program communication is provided through the HP-30003-60013 Control Panel and System Console.

II. MINI-OPERATING INSTRUCTIONS

A. Operations

1. Cold-Load HP-30030B/C Selector Channel Diagnostic File # (number associated with D429A) from the Non-CPU Cold-Load Tape.

2. Respond to Speed-Sense by asserting "CR" at the System Console.

3. Respond, where necessary, to the dialogue at the System Console.

B. Switch-Register Options

SWITCH	FUNCTION
0	SELECT EXTERNAL SWITCH REGISTER
1	SET TO CHANGE SECTION SELECT REGISTER
2	SPARE
3	SPARE
4	SPARE
5	LOOP CURRENT SECTION
6	RUN ON MUX MODE (FOR SCMB VERIFICATION ONLY. REFER TO MESSAGE Q104)
7	OUTPUT TO LINE PRINTER (IF CONFIGURED IN SDUP)
8	SPARE
9	SUPPRESS NON-ERROR MESSAGES
10	SUPPRESS ERROR MESSAGES
11	LOOP ON LAST STEP
12	HALT ON ERROR
13	HALT AT END OF STEP
14	HALT AT END OF SECTION
15	HALT AFTER COMPLETE PROGRAM CYCLE

C. Section Switch-Register Options

BIT	SECTION
0	RE-CONFIGURE
1	SELECT SECTION 1
2	SELECT SECTION 2
3	SELECT SECTION 3
4	SELECT SECTION 4
5	SELECT SECTION 5
6	SELECT SECTION 6
7	SELECT SECTION 7
8-15	SPARE

II. MINI-OPERATING INSTRUCTIONS (continued)

D. Halt Assignments

NO. (OCTAL)	FUNCTION
0	HALT FOR EXTERNAL SW. REG.
1	HALT FOR SECTION SWITCH REG.
2	HALT TO RESTORE EXTERNAL SWITCH REG.
3	HALT ON ERROR COUNT REACHED
4-11	SPARE
12	HALT ON ERROR
13	HALT AFTER STEP
14	HALT AFTER SECTION
15	HALT AFTER COMPLETE PROGRAM CYCLE
16-17	SPARE

III. REQUIREMENTS

A. Hardware

The hardware configuration required for this test is a minimum HP 3000 Series II or Series III Computer System with the Selector Channel and a HP 30033A SCMB. Refer to System Service Manual Section IV for SCMB installation procedure and to Section I for verification procedure for the SCMB.

B. Software

The Stand-Alone Diagnostic Utility Program (SDUP) is required to create the Stand-Alone Diagnostic tape. The tape is comprised of Cold-Load program, the Relocating Loader, and one or more diagnostic programs including the Stand-Alone HP 30030B/C Selector Channel Diagnostic program. All the programs are coded in System Programing Language (SPL/3000).

IV. DETAILED OPERATING INSTRUCTIONS

A. Operating Instructions

The following are the instructions for loading, executing, and configuring the Stand-Alone HP 30030B/C Selector Channel Test program.

1. Cold-Load by entering %3006 into the Switch-Register and simultaneously depress "LOAD" and "ENABLE" switch on the CPU Front Panel.

2. Select an appropriate Diagnostic File # (associated with the HP 30030B Selector Channel Diagnostic) and enter that number into the Switch-Register. Depress "RUN" switch. The diagnostic tape supplied is identified by file names and their respective file position on the tape.

3. The diagnostic program is now executable.

4. Depress "CR" key on the System Console to respond to the Speed-Sense. The program, then, prints the diagnostic header information and requests necessary parameters to begin the diagnostic cycle.

B. Options

Under HP 30030B/C Selector Channel Test, the operator can control halts after sections, or steps or upon program completion. Control suppression of error and non-error messages; and control test loop on a specific step. These control options may be entered when the program requests for a specific option entry via the test dialogue.

It should be noted, however, that the test program has been pre-configured to be executable in its best load and go configuration.

1. The options available in Section II.B are applicable to the program inquiring of the type:

Q104 SELECT OPTIONS

The description of the usage of bits (Ø and 1) under the option in Section II.B is as follows:

BIT #Ø	Bit #1	Function
Ø	Ø	Uses previously configured value.
Ø	1	Uses previously configured value.
1	Ø	The program will not give the option to re-configure and it will use the currently selected values in the Switch Register as an external switch register option and it will continue to execute until current register value is changed.
1	1	If this option is selected, it suggests possible reconfiguration (see bit Ø of Section IV.B.2).

2. The following describes the options associated with each bit of the Section Select Switch Register for the program request of the following message:

   "Q11Ø SELECT SECTION OPTIONS"

   (Same options as those described in Section II.C)

   If bit Ø is not selected (Ø), the program continues execution using previously configured values.

   If bit Ø is selected (1), the program requests restoration of External Switch-Register Options, device# (DRT#) for the Selector Channel Maintenance Card (decimal), Upper Bank# configured (decimal), Upper Address Configured (octal) (does not ask for upper address if running the HP 30030B), and the error print# (octal).

3. The options available in Section II.B are applicable to the program inquiry of the message type:

   "Q111 RESTORE SELECT OPTIONS"

   This message is yield only after an option bit Ø in Section II.C is selected. The bit Ø and bit 1 functions are same as that described in Section IV.B.1 with the exception of (1Ø) combination. The difference, when bit Ø is a logical 1 and bit 1 is a logical Ø, in this case is in addition to using the currently selected value in the Switch Register as an external switch register value the program will make further inquiries before going into a continuous execution.

C. Halts and Message Tables

When a program halts, an instruction is displayed in the Current Instruction Register (CIR) of the 3ØØØ3-6ØØ13 Control Panel. The register is displayed as: (Ø Ø11 ØØØ Ø11 11X XXX), where X's is the Halt# (octal).

See Halt Assignment table as described in Section II.D.

1. Message Formats - There are basically four types of message classificiations: D, E, P, and Q classes.

   D - Class: Messages which describe program boundaries. Some operator intervention is necessary.

   E - Class: Messages related to error or step number. Some operator intervention is necessary.

   P - Class: Messages which describe the test completion of a Section, step, or an indication for a certain tested properties. Some operator intervention is necessary.

   Q - Class: Inquiry messages by the program for the parameter entry. An operator intervention is required.

2.1 MESSAGE DESCRIPTOR

2.1.1 D1ØØ HP-30030B/C SELECTOR CHANNEL DIAG. (D429X.YY.ZZ)
: This is the header information for this diagnostic program;

Where

X = Version Number
YY = Update Number
ZZ = Fix Number

2.1.2 D11Ø DIRECT I/O TEST
: This message indicates that the test is now in execution for CIO, TIO, WIO, RIO and SIN I/O command test.

2.1.3 D127 DIRECT I/O TEST COMPLETED
: This message indicates that the test has been completed for the Direct I/O Commands.

2.1.4 D130 CONTROL ORDER TEST
: This message indicates that the test is now in execution for all Selector Channel SIO (START I/O) orders except READ and WRITE orders.

2.1.5 D217 CONTROL ORDER TEST COMPLETE
: This message indicates that the test has been completed for Control Order Test.

2.1.6 D22Ø READ TEST
: This message indicates that the test has begun for Read Order Test.

2.1.7 D244 2K READ X MILLISEC; BANK Y
: This message indicates that the transfer time for 2K Read from Bank Y is X milliseconds.

2.1.8 D247 READ TEST COMPLETED
: This message indicates that the Read Order Test has been completed.

2.1.9 D25Ø WRITE TEST
: This message indicates that the test is now in execution for Write Order Test.

2.1.10 D274 2K WRITE X MILLISEC; BANK Y
: This message indicates that the transfer time for 2K Write to Bank Y is X milliseconds.

2.1.11 D275 WRITE TEST COMPLETED
: This message indicates that the Write Order Test has been completed.

2.1.12 D3ØØ CHAIN READ TEST
: This message indicates that the test is now in execution for a chained Read Order Test.

2.1.13 D317 CHAINED READ TEST COMPLETED
: This message indicates that the Chained Read Test has been completed.

MESSAGE DESCRIPTOR (continued)

2.1.14 D32Ø CHAINED WRITE TEST
: This message indicates that the test is now in execution for a chained Write Order Test.

2.1.15 D337 CHAINED WRITE TEST COMPLETED
: This message indicates that the Chained Write Order Test has been completed.

2.1.16 D34Ø ERROR RESPONSE TEST
: This message indicates that the test is now in execution for an Error Response Test.

2.1.17 D367 ERROR RESPONSE TEST COMPLETE
: This message indicates that the Error Response Test has been completed.

2.1.18 D6ØØ CHANNEL DIAG. COMPLETE
: This message indicates that the selected test section(s) has been completed one pass.

2.1.19 D6Ø1 END OF PASS X
: This message indicates that the diagnostic test has completed X passes for those test sections selected.

2.1.20 Q1Ø4 SELECT OPTIONS
: This message indicates that the program is requesting any of the option entry available and described in Section II.B.

The options available in Section II.B are very much self-explanatory with the exception of option for bit 6. When bit 6 is selected, insure that the jumper is in the MUX MODE on the Selector Channel Maintenance Board. To verify operation of the SCMB, put jumper in MX, install SCMB in MUX channel and run the Selector Channel Diagnostic (D429). Refer to System Service Manual, Section IV for additional details. It should be noted that not all tests are executed under Mux Mode.

2.1.21 Q11Ø SELECT SECTION OPTIONS
: This message indicates that the program is requesting any of the option entries available and described in Section II.C.

2.1.22 Q111 RESTORE SELECT OPTIONS
: This message indicates that the program is requesting any of the option entries available and described in Section II.B.

2.1.23 Q1Ø1 SET MAINT. CARD DEV NUM?
: This message indicates that the program is requesting a device number for the Selector Channel Maintenance Board. The device number must be specified in decimal and its range is:

(3≤ DEVICE ≤ 127)

2.1.24 Q1Ø2 TIMER/CONSOLE DEV NUM?
: This message indicates that the program is requesting the CLOCK/TTY device number. The device number must be in decimal and its range is:

(3≤ DEVICE ≤ 127)

2.1.25 Q1Ø8 ENTER UPPER BANK# (DECIMAL)=
: This message requests the highest bank number for the memory as configured currently. This input must be specified in decimal and its range is: (Ø ≤ Bank ≤3) for HP 30030B or (Ø ≤ Bank ≤ 15) for HP 30030C.

2.1.26 Q1Ø9 ENTER UPPER ADDRESS (OCTAL) =
: This message requests the highest address (octal) that is addressable for the memory bank specified in Section IV.C.2.1.25. This question is asked only if running THE HP 30030B; specify bank and upper address for the various memory sizes as follows:

Memory Size (Wds)	Bank	Address
64K	Ø	% 177777
96K	1	% Ø77777
128K	1	% 177777
16ØK	2	% Ø77777
192K	2	% 177777
224K	3	% Ø77777
256K	3	% 177777

2.1.27 Q1Ø5 ERR PRINT LIMIT?
: This message indicates that the program is requesting the maximum error count number. The number is specified in octal and its range is:

(Ø ≤ COUNT ≤ 7777_8).

3.0 DIAGNOSTIC MESSAGES

STEP [MESSAGE]	COMMENT
D100 HP 30030B/C SELECTOR CHANNEL DIAG (D429)	Title message printed after program is loaded.
Q101 SET MAINT CARD DEV NUM?	Enter the decimal device number of Selector Channel Maintenance board on the console followed by a CR/LF.
Q102 SET TIMER/CONSOLE DEV NUM?	Enter the decimal device number of System Timer and Console Interface Board on the systems console followed by a CR/LF.
Q104 SELECT OPTIONS	Set switch register to desired options (sec. II.B) and press RUN.
Q105 ERR PRINT LIMIT?	Enter error count. (MAX: 7777_8)
Q108 ENTER UPPER BANK# (DECIMAL)=	Enter upper bank# (decimal) & press CR/LF.
Q109 ENTER UPPER ADDRESS (OCTAL)=	Enter upper address (octal) for the bank# entered.
Q110 SELECT SECTION OPTIONS	Enter appropriate bit(s) from II.C and depress RUN.
Q111 RESTORE SELECT OPTIONS	Enter appropriate bit(s) from II.B and depress RUN.
D110 DIRECT I/O TEST	Section 1 identification.
E111 CIO FAILED, TEST ABORTED	Direct CIO instruction failed and the remainder of the diagnostic is aborted. (The error messages of this section, E111 through E116, will probably be preceded by one of the general error messages, E500 through E520, applicable to all sections.)
E112 TIO FAILED, TEST ABORTED	Direct TIO instruction failed and remainder of diagnostic is aborted.
E113 WIO FAILED, TEST ABORTED	Direct WIO instruction failed and remainder of diagnostic is aborted.
E114 RIO FAILED, TEST ABORTED	Direct RIO instruction failed and remainder of diagnostic is aborted.
E115 CIO FAILED, TEST ABORTED	Direct CIO instruction failed and remainder of diagnostic is aborted. Note that the TIO instruction could be at fault here. The order of execution following the previous RIO is TIO, CIO, TIO, with the final status returned being compared against the expected status and the first TIO status.

DIAGNOSTIC MESSAGES (continued)

STEP [MESSAGE]	COMMENT
E116 SIN FAILED	Direct SIN instruction failed.
D127 DIRECT I/O TEST COMPLETED	Section 1 completed.
D130 CONTROL ORDERS TEST	Section 2 indentification.
131	Setup and execute SIO program to "jump on self".
132	Execute CIO instruction to clear interface.
133	Check status, confirm SIO OK bit high. An error will produce message E515.
E134 IMPROPER TERM, SIO PGM COMPLETED	Expects SIO program to terminate and not complete. If it completes, it indicates that the unconditional JUMP order probably failed.
135	Check DRT properly restored and pointing to expected address. An error will produce message E517.
140	Set up SIO program consisting of END order without interrupt and execute.
E141 STATUS NOT RETURNED	Indicates status not returned following SIO's END order. If returned status is incorrect then an E515 message (Status Error) will be printed.
142	Executes direct TIO and compares actual status against that predicted. An error result is message E515.
143	Check DRT properly restored and pointing to expected address. An error will produce message E517.
144	Set up SIO program consisting of END order with interrupt request set and execute.
145	Check for interrupt. If no interrupt is received, message E503 is output.
E146 STATUS NOT RETURNED	Indicates status not returned following SIO's END order. If returned status is incorrect, then an E515 message will be output.

DIAGNOSTIC MESSAGES (continued)

STEP [MESSAGE]	COMMENT
147	Executes direct TIO and compares actual status against that predicted. An error results in message E515.
150	Check DRT properly restored and pointing to expected address. An error will produce message E517.
155	Set up and execute SIO program with INTERRUPT order.
156	Check for interrupt. No interrupt generates error message E503.
E157 SIO PGM DID NOT COMPLETE	Checks for SIO program completion and checks status. If status is in error, then message E515 is output.
160	Set up and execute SIO program with SENSE order.
161	Check status returned from SENSE order. If status is in error message, E515 will be output. If actual status (in message E515) is all 1's, then no status was returned.
162	Check status returned with END order. Again, message E515 will be output if status is in error and 'actual' will be all 1's if no status returned.
170	Set up SIO program with consecutive SENSE orders at absolute addresses %77776 and %1ØØØØØ and execute.
E171 ADDRESS ROLLOVER FAILED	This message indicates that second SENSE order, at absolute address %1ØØØØØ, did not execute. If returned status is other than that predicted, then message E515 is output.
172	Set up and execute unconditional JUMP order to address X where a SENSE order is executed followed by another unconditional JUMP to the 1's complement of X.

STEP [MESSAGE]	COMMENT
173	Checks first jump location by examining status returned by SENSE order. If in error, then message E515 is generated. If "ACT" status in message E515 is all Ø's, then jump probably failed.
174	Checks second jump location by examining status returned by END order in a manner analogous to that of the preceding step.
175	Set up and execute conditional JUMP order with JUMP MET bit off.
E176 ILLEGAL JUMP	Output if JUMP order executed, it should have been treated as a NO-OP.
200	Set up and execute conditional JUMP order with JUMP MET bit on. A jump to address X should occur where a SENSE order is executed followed by another conditional JUMP to the 1's complement of X.
201	Checks first jump location by examining status returned by SENSE order. If in error, then message E515 is generated. If "ACT" status in message E515 is all Ø's, then jump probably failed.
202	Checks second jump location by examining status returned by END order in a manner analogous to that of the preceding step.
203	Transmit direct CIO with control code set to load IOCW.
204	Set up and execute SIO program consisting of CONTROL and END orders.
E205 IOCW LOAD ERR EXP XXXXXX ACT YYYYYY	This message is output if IOCW is loaded incorrectly. The expected and actual IOCW of Step 204 is also printed.
206	Execute SIO programs of step 204 but with 1's complement of bits 5-15 of IOCW.
E207 IOCW LOAD ERR EXP XXXXXX ACT YYYYYY	This message is output if IOCW is loaded incorrectly. The expected and actual IOCW of Step 206 is also printed.

DIAGNOSTIC MESSAGES (continued)

STEP [MESSAGE]	COMMENT
210	Transmit direct CIO with control code set to load IOAW.
211	Set up and execute SIO program consisting of CONTROL and END orders.
E212 IOAW LOAD ERR EXP XXXXXX ACT YYYYYY	This message is output if IOAW is loaded incorrectly. The expected and actual IOAW of Step 211 is also printed.
213	Execute SIO program of step 211 but with 1's complement of IOAW.
E214 IOAW LOAD ERR EXP XXXXXX ACT YYYYYY	This message is output if IOAW is loaded incorrectly. The expected and actual IOAW of Step 213 is also printed.
D217 CONTROL ORDERS TEST COMPLETED	Section 2 completed.
D220 READ TEST	Section 3 identification.
221	Issues direct WIO command to fill buffer with data pattern.
222	Set up and execute SIO program to read 2 words (for both buffers).
223	Checks READ order execution by examining status, data read, and DRT properly restored (IOAW incrementing) and if any, or all, are in error generates message E515, E516, or E517 respectively. The program then loops back to STEP 221 several times to vary the data pattern and location of SIO program execution.
225	Set up SIO program to transfer up to 4K word blocks with control code set to count either TIX, RNW, RS, or EOT's.
226	Read and count signal. Check for proper number and loop back to STEP 225 until all signals are counted. If an error is detected, the appropriate error message [E506-E511] will be generated.
230	Issues direct WIO command to fill buffer with data pattern.

STEP [MESSAGE]	COMMENT
231	Set up and execute SIO program to read 2 words (for both buffers) with the FAST SERVICE REQUEST bit set.
232	Checks READ order execution by examining status, data read, and DRT properly restored (IOAW incrementing) in FAST SR mode of operation. If any, or all, are in error, message E515, E516, or E517 respectively are generated. The program then loops back to STEP 230 several times to vary the data pattern and location of SIO program execution.
235	Set up SIO program to transfer up to 2K words in FAST SR mode with control code set to count either TIX, RNW, RS, or EOT's.
236	Read and count signals. Check for proper number and loop back to STEP 235 until all signals are checked, If an error is detected the appropriate error message [E506-E511] will be generated.
240	Set up SIO program for READ with Immediate Device End (IDE) bit set in control word and execute.
E241 IDE FAILED;ADR %XXXXXX; BANK XX (XX = 00 - 03)	Checks that no read occurred. IDE should have caused it to fall through. If not, this error message is output.
242	Set up SIO program for READ of up to 4K word with Terminate on Terminal Count (TTC) bit set in control word and execute.
E243 TTC FAILED AT XXXX; ADR %XXXXXX; BANK XX	Checks that TTC did, in fact, terminate the read. If not, then this error message is output where XXXX is where counter rollover and terminations should have occurred. If the READ order terminated correctly, then the RETURN RESIDUE count is checked. If this is in error, message E520 is generated. The program then loops back to STEP 242 several times to test different TTC counts and RESIDUE counts.
D244 2K READ XXXX MILLISEC: BANK X (X = 0 - 3)	Time required for last 2K read in milliseconds.

STEP[MESSAGE]	COMMENT
D247 READ TEST COMPLETED	Section 3 completed.
D250 WRITE TEST	Section 4 identification.
251	Set up SIO program and write a word.
252	Issue direct RIO to read word back.
253	Check input. Check both status and data and if either is in error, output message E515 or E516 respectively. The program then loops back to STEP 251 several times to vary the data pattern tested.
255	Set up SIO program to transfer up to 4K words with control code set to count either TOX, WS, or EOT's, or with TNC (Terminate on No Compare) set.
256	Count signals. Check for proper number and loop back to STEP 255 until all signals are counted. If an error is detected, the appropriate error message (E511-E516) will be generated.
260	Set up SIO program with FAST bit set in control word and issue WRITE order.
261	Issue direct RIO to read word back.
262	Checks WRITE order execution by examining status and data read back in FAST SR mode of operation. If either is in error, then message E515 or E516 respectively will be generated. The program then loops back to STEP 260 several times to vary the data pattern.
265	Set up and execute SIO program to transfer up to 2K words in the FAST SR mode with the control code set to count either TOX, P WR STB, or EOT's, or with TNC (Terminate on No Compare) set.
266	Count signals. Check for proper number and loop back to STEP 265 until all signals are checked. If an error is detected, the appropriate error message (E511-E516) will be generated.
270	Set up and execute SIO programs for WRITE with IDE bit set in control word.
E271 IDE FAILED; BANK XX	Issues direct RIO to confirm that no WRITE occurred. If SIO program did not fall through, then this error message is generated.

DIAGNOSTIC MESSAGES (continued)

STEP[MESSAGE]	COMMENT
272	Set up SIO program for WRITE of up to 4K words with Terminate on Terminal Count (TTC) bit set in control word and execute.
E273 TTC FAILED AT XXXX	Checks that TTC did, in fact, terminate the WRITE by executing a direct RIO. If not, then this error message is output where XXXX is where counter rollover and termination should have occurred. If the WRITE order terminated correctly, then the RETURN RESIDUE count is checked. If this is in error, message E520 is generated. The program then loops back to STEP 272 several times to test different TTC counts and RESIDUE counts.
D274 2K WRITE XXXX MILLISEC; BANK X	Times the last 2K WRITE executed and prints the time in milliseconds.
D275 WRITE TEST COMPLETED	Section 4 completed.
D300 CHAINED READ TEST	Section 5 identification.
301	Set up and execute SIO program to perform one or more chained READ's in the SLOW SR mode.
E302 DATA GAP AT XXXXXX; BANK XX	Checks operation of chained READ order. First checks returned status and issues error message E515 if warranted. Next it looks for data gaps between chained READ orders and outputs the message associated with this step number if an error is detected, where XXXXXX is the absolute address where the gap begins. Also checked is data read, returned residue, and counts made of TIX's, LOT's, RNW's, and RD STRBS. If any errors are recognized with the above, their respective error message is generated. The program then loops back to STEP 301 several times to vary the READ orders.
304	Issues direct WIO to fill buffer. This is used to force a clear interface with TTC set during a block transfer to check order prefetch.
305	Set up and execute SIO program with chained READ orders in the SLOW SR mode.

DIAGNOSTIC MESSAGES (continued)

STEP[MESSAGE]	COMMENT
E306 PREFETCH FAILED, TC X	Prefetch should complete. If not, this message is output. The program then loops back to STEP 304 several times to check the prefetch at both 4 word and 2K word chained READ's. TC means Test Count and X is either 4 or 2K to indicate where the prefetch was checked. Status and RESIDUE is also checked.
310	Set up and execute SIO program to perform one or more chained READ's in the FAST SR mode.
E311 DATA GAP AT XXXXXX; BANK XX	Checks operation of chained READ. The program first examines the returned status and if in error generates message E515. Next it looks for data gaps between chained READ orders and outputs the message associated with this step number if an error is detected, where BANKAH-%500 is the absolute address where the gap begins. Also checked is data read, returned residue, and counts made of TIX's, EOT's, RNW's, and RD STRB's. If any errors are detected in the above, there respective error message is generated. The program then loops back to STEP 310 several times to vary the READ orders.
313	Issue direct I/O command to fill buffer with TTC count. This is used to force a clear interface during a block transfer to check order prefetch.
314	Set up and execute SIO program with chained READ orders in the FAST SR mode.
E315 PREFETCH FAILED, TC X; BANK XX	IOAW should not get prefetched but IOCW should. This message is output if the prefetch is in error and then loops back to STEP 313 several times. TC means Test Count, set in step 313, and X is either 4 or 2K. to indicate where the prefetch was checked. STATUS is also checked.
D317 CHAINED READ TEST COMPLETE	Section 5 completed.
D320 CHAINED WRITE TEST	Section 6 identification.
321	Set up and execute SIO program to perform one or more chained WRITE's in the SLOW SR mode.
322	Checks operation of chained WRITE order. Examines status, data order, and returned residue and generates message E515, E516, or E517 respectively if any are in error. Also, a count is made of the signals TOX, EOT, and WT STRB's and their respective error message is generated if warranted. The program then loops back to STEP 321 several times to vary the WRITE orders.

STEP[MESSAGE]	COMMENT
324	Issues direct I/O command to fill test boards buffer with Terminal Count. This is used to force a clear interface during the block transfer (which follows) to check order prefetch.
325	Set up and execute SIO program with chained WRITE orders in the SLOW SR mode.
E326 PREFETCH FAILED, TC X ; BANK XX	Prefetch should complete if at least 5 words are written. If not, this message is output where TC means Test Count and X is between 4 and 2K to indicate where the prefetch was checked. The program then loops back to STEP 324 several times. Status is also checked on each pass.
330	Set up and execute SIO program to perform one or more chained WRITE orders in the FAST SR mode.
331	Checks operation of chained WRITE order. Examines status, data order, and returned residue and generates message E515, E516, or E517 respectively if any are in error. Also, a count is made of the signals TDX, EOT, and WT STRB's and their respective error message is generated if warranted. The program then loops back to STEP 330 several times to vary the WRITE orders.
333	Issues direct I/O command to fill test boards buffer with Terminal Count. This is used to force a clear interface during the block transfer (which follows) to check order prefetch.
334	Set up and execute SIO program with chained WRITE orders in the FAST SR mode.
E335 PREFETCH FAILED, TC X; BANK XX	Neither IOCW or IOAW should be prefetched. If in error, this message is output where TC means Test Count and X is between 4 and 2K to indicate where the prefetch was checked. The program then loops back to STEP 333 several times. Status is also checked on each pass.
D337 CHAINED WRITE TEST COMPLETED	Section 6 completed.
D340 ERROR RESPONSE TEST	Section 7 identification.
341	Issue direct WIO to set false DRT# into buffer.

DIAGNOSTIC MESSAGES (continued)

STEP[MESSAGE]	COMMENT
342	Set up and execute SIO program using READ orders and the DRT # set in STEP 341.
343	Check data response and generate message E516 if in error. Also checks device status. The program then loops back to STEP 341 several times to vary the DRT #.
344	Set up and execute SIO program to access the 8K block of core below the limit indicated in STEP 103.
E345 MEM REPORTS NOT PRESENT; BANK XX	This message is output if the SIO program could not access memory. Status is also checked and its error message (E515) should also be output if memory could not be accessed.
346	Set up and execute SIO programs to access the 8K block of core above the limit indicated in STEP 103 if the limit is less than 64.
E347 MEM REPORTS PRESENT	This message is output if the program behaved as if memory were present. Status is also checked and its error message (E515) will be output, if in error.
350	Set up SIO program for Service Out (SO) time-out and execute.
E351 NO SO TIMEOUT; BANK XX	This message is generated if SO didn't timeout. (Channel acknowledge not returned within 10 microseconds.)
352	Set up SIO program for Service Request (SR) timeout using READ orders and execute.
E353 NO SR TIMEOUT; BANK XX	This message is generated if SR didn't timeout. (No SR within 1000 milliseconds after READ.)
354	Set up SIO program for SR timeout using WRITE orders and execute.
E355 NO SR TIMEOUT;BANK XX	This message is generated if SR did not timeout.
360	Set up and execute SIO program with illegal program orders consisting of Data Chain (DC) bit set and ORDER other than READ or WRITE.
E361 NO ERR WITH DC 1, ORDER XXX	Should have received a transfer error. If not, this message is output. The X's refer to the ORDER code and will be either 001 (RESIDUE), 011 (END), or 101 (SENSE).
362	Set up and execute SIO program consisting of either the illegal code chained READ order followed by a SENSE order or chained WRITE order followed by a SENSE order.

DIAGNOSTIC MESSAGES (continued)

STEP [MESSAGE]	COMMENT
L363 NO ERR WITH CHAINED XX/SENSE	This message is output if no error was recognized in the preceding SIO program. The XX will be either RD for READ or WT for WRITE. If the expected status and actual status do not agree (expect XFER ERR) then message E515 is also output. The program then loops back to STEP 362 to execute both orders.
D367 ERROR RESPONSE TEST COMPLETED	Section 7 completed.
P465 END OF STEP XXX	Printed prior to halt of switch 13 set.

NOTE: Messages E500 to E520 which follow are general error messages and may be associated with any of the previous STEPS.

E500 NON-RESP DEV CNTLR IN STEP XXX	Condition code of CCL returned when I/O operation tried.
E501 DEVICE NOT READY IN STEP XXX	Device indicates NOT READY when I/O operation tried.
E502 ILLEGAL COND-CODE IN STEP XXX	A condition code of CCG or NUL was returned.
E503 NO INTERRUPT IN STEP XXX	An expected interrupt did not occur.
E504 UNEXPECTED INTERRUPT IN STEP XXX	Received an unexpected interrupt.
E506 TIX COUNT ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Count of TIX (Toggle In Transfer) signals in error.
E507 RNW COUNT ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Count of RNW (Read Next Word) signals in error.
E510 RS COUNT ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Count on RS (Read Strobes) signals in error.
E511 EOT COUNT ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Count of EOT (End of Transmission) signals in error.

DIAGNOSTIC MESSAGES (continued)

STEP [MESSAGE]	COMMENT
E512 TOX COUNT ERR IN STEP XXX; ADR%XXXXXX;BANK X EXP XXXXXX ACT XXXXXX	Count of TOX (Toggle out Transfers) signals in error.
E513 WS COUNT ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Count of WS (Write Strobe) signals in error.
E515 STATUS ERR IN STEP XX EXP XXXXXX ACT XXXXXX	Expected and Actual Status do not agree.
E516 DATA ERR IN STEP XXX; ADR%XXXXXX; BANK X EXP XXXXXX ACT XXXXXX	Data error detected in transfer. Note that in large word transfers, this message printing would become prohibitive, therefore, under these conditions the operator should set switch 10 or switch 7 with bit Ø up.
E517 DRT NOT RESTORED CORRECTLY IN STEP XXX; BANK XX EXP ADR XXXXXX ACT ADR XXXXXX	Indicates that the expected DRT address pointer was not restored.
E520 RESIDUE ERR INSTEP XXX; BANK XX EXP XXXXXX ACT XXXXXX	Returned RESIDUE was other than expected.
D600 SELECTOR CHANNEL DIAG COMPLETED	Diagnostic completion message.
D601 END OF PASS XX	Indicates number of passes through program.

D. Pre-Configuration Option

The HP 30030B/C Selector Channel Diagnostic program has been configured to execute in best load and go configuration using the options available from Section II.B and II.C. The pre-configured values can be modified at the time when the cold-load tape is being generated under SDUP (System Diagnostic Utility Program).

The following are the DB locations containing data that can be changed during pre-configuration.

DB+0 Switch Register Setting
DB+1 Section Register Setting
DB+2 Version and Update Level
DB+3 SCMB DRT number
DB+4 Maximum Error Print Count
DB+5 Clock/Console IF DRT number
DB+6 Upper Bank number 0 to 3 maximum for HP 30030B; Ø to 15 (decimal) maximum for HP 30030C
DB+7 Upper Bank Address (Refer to message Q109)

E. Control and Status Words

1. HP 30033A Selector Channel Maintenance Board

1.1 Control Word Format

MR	RI	JM	IDE	TA	TS	CONTROL CODE		F	SDN	TTC	TNC	CLR IL	COUNT CODE		
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit#

0 MASTER RESET - issues a programmed I/O reset which clears the maintenance card, including the control register and data buffer, and sends clear interface to the channel if the channel is active.

1 RESET INTERRUPT - clears the interrupt request flip flop.

2 JUMP MET - sets condition met for conditional jumps.

3 IMMEDIATE DEVICE END - forces device end at the beginning of any data transfer on the selector channel. No effect on the multiplexer channel.

4 TIMEOUT ACKNOWLEDGE - causes channel acknowledge to be inhibited following the current control order. Any subsequent channel service out will timeout. The selector channel will restore the DRT pointer, but no clear interface will occur. The maintenance card will remain busy until a direct master reset is issued. The multiplexer channel ignores this control bit.

1.1 Control Word Format (continued)

5 TIMEOUT SERVICE REQUEST - inhibits device service request after the current control order. The selector channel will issue a clear interface, forcing an interrupt, and restore the DRT pointer. The multiplexer channel program will simply stop, and no interrupt will be issued.

6:7 CONTROL CODE - defines how SIO program control orders will be treated.

00 - Ignore IOCW, use IOAW as a control word (default).

01 - Load IOCW into data buffer only (the control register is unchanged).

10 - Load IOAW into data buffer only.

11 - Load IOCW, then IOAW into data buffer.

8 FAST BIT - overrides normal data service request delay (5 μs → 200 KHz) to force continuous service requests in data transfers.

9 SPECIAL DEVICE NUMBER - specifies that the maintenance card, when asked to supply its device number, will gate out bits 8:15 of its data buffer, allowing the card to simulate any device number in running SIO programs. Interrupts and direct commands will continue to correspond to the hardwired device number.

10 TERMINATE ON TERMINAL COUNT - specifies that counter rollover will terminate the current data transfer by device end (selector channel only) or clear interface (both) depending on bit 12.

11 TERMINATE ON NO COMPARE - enables a comparator and disables counter/buffer loading by programmed write strobes. Data sent to the card is compared with the current buffer contents, and a compare failure will terminate the transfer by device end (selector channel only) or clear interface (both) depending on bit 12.

12 CLEAR INTERFACE - specifies that a clear interface, rather than the default device end, should be issued if either or both of the above termination tests is met.

13:15 COUNT CODE - controls the counter/buffer. The normal mode is NOP, i.e., no counter, buffer operation only. Codes are as follows:

000	NOP	100	P WR STB
001	READ NEXT WORD	101	TOGGLE OUT XFER
010	P RD STB	110	EOT
011	TOGGLE IN XFER	111	CHANNEL SO

1.1 Control Word Format (continued)

Octal codes 1 to 7 specify that the counter will be incremented by the occurrence of the selected signal. Codes 4 to 7 inhibit loading of the counter/buffer to preserve the count. Code 7 (count channel service out) should not be issued by an SIO control order since there is a timing ambiguity as to whether the current cycle itself should be counted.

1.2 Status Word Format

SIO OK	R/W OK	INT BLQ	INTXFER ACTERR		ENB	DEV END	EOT	NC	TC	INX	OUTX	CLR IL	0	
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15

The status word is returned by a direct TIO or by a P SENSE STB. Reading status does not in itself change any of the test board states. As indicated below, certain transfer related status bits are cleared by direct SIO or channel directives to begin a new transfer.

0 SIO OK - True if the channel is inactive and the test board is not currently executing an SIO program.

1 READ/WRITE OK - Always true.

2 INTERRUPT REQUEST - True if the test board is currently interrupt requesting for any reason.

3 INTERRUPT ACTIVE - True if the test board interrupt circuit is currently in the active state.

4 TRANSFER ERROR - True if the channel has sent transfer error to the test board. Cleared by the next SIO or reset.

5 ENABLE True if the channel is inactive. This is a positive true version of the "ENABLE" signal from the channel.

6 DEVICE END - True if the test board has issued device end. This bit is cleared at the beginning of a new transfer, by SIO and by reset.

7 EOT - True if the channel has asserted EOT (end of transfer). Cleared by the beginning of a new transfer, by SIO and by reset.

8:9 NO COMPARE and TERMINAL COUNT flip flops - Set if the respective condition has occurred. Cleared by SIO, reset, or the beginning of a new transfer.

1.2 Status Word Format (continued)

10:11 IN TRANSFER and OUT TRANSFER flip flops - Indicate the state of the bus logic flip flops, one of which will be set by the channel during data transfers (READ = INBOUND, WRITE = OUTBOUND).

12 CLEAR INTERFACE - Set if the test board has issued clear interface to the channel. Cleared by SIO or reset.

13:15 Currently unassigned (zero).

V. DETAILED TEST DESCRIPTION

The Stand-Alone HP 30030B Selector Channel Diagnostic Program is composed of seven (7) test sections. The test description per section is given as follows:

1.0 Direct I/O Verification Test

A cursory check of the HP 30033A Selector Channel Maintenance Card is performed in this section by using the Direct I/O commands CIO, TIO, WIO, RIO and SIN. These commands communicate with the maintenance card via the I/O Processor and IOP Bus, completely bypassing the selector channel and its Port Controller. Since it is assumed that a minimum system is present and operational if any of these commands fail, an error message will be output on the system's console and, except for a failing SIN instruction, the remainder of the program will be aborted.

The steps in this section are numbered from 110 to 127 and are executed by setting the Section Select Switch to 1.

2.0 Control Orders, SIO Program Responses Except Read/Write

This section tests all Selector Channel SIO (Start I/O) program responses except Read and Write Orders. The ability to "free" a "stuck" channel is checked first in case its use should become necessary later in the program.

Initially an SIO program will be set up consisting of an unconditional JUMP order to jump on itself. This should "hang-up" the channel. A direct CIO to clear interface logic (CLRIL) will then be issued to clear the channel. The checks that follow include confirming that the SIO OK bit is set, that the jump instruction performed correctly, and that the DRT is properly restored and pointing at the predicted location. This procedure will be used throughout the program to clear a channel that is suspected of being "hung-up".

2.0 Control Orders, SIO Program Responses Except Read/Write (continued)

The END order is checked next, both with and without interrupt request set. An SIO program is constructed consisting of a CONTROL and an END order without interrupt. After execution, a check is made for the SIO OK bit set, the DRT properly restored, and status returned following the END order. If the above is successful the procedure is repeated with the END order requesting an interrupt and a check for its occurrence.

SIO programs are set-up next to test the INTERRUPT and SENSE orders respectively. Following the INTERRUPT Order, a check is made for proper I/O program termination.

After the SENSE order has been checked, a test is performed to confirm that the IOPCNT is properly incrementing and that address rollover functions correctly. To accomplish this, several SENSE orders will be executed around the absolute address boundary %77700 to %100020.

Both conditional and unconditional jumps are tested next. First, an unconditional JUMP to some address, call it X, will be executed. At that address there will be a SENSE order, to determine if the JUMP was good, followed by another unconditional JUMP to an END order at the 1's complement of X. The same procedure is executed again using the conditional JUMP command. In addition, the conditional JUMP order is also checked for FALSE if the JUMP MET bit is clear.

The last SIO Program order to be tested in this section is the CONTROL order. Using the Control Code (bits 6 & 7) of the Direct CIO command, the SIO programs control order will load either the IOCW or the IOAW into the data buffer. All bits of both words (except 0-4 of the IOCW) will be tested high and low to insure bit integrity.

The steps in this section are numbered from 130 to 217 and are executed by setting the Section Select Switch to 2.

3.0 Read Order Test, No-Chaining

This section tests the SIO's READ order both with and without the RETURN RESIDUE order and DEVICE END set. Initially a WIO command is issued to fill the maintenance cards buffer, followed by two consecutive SIO programmed READ orders to check both input buffers in the selector channel. The buffer pointer is checked by insuring that the data is input in the proper order. The status word is also checked to insure that the IN XFER (In Transfer) bit is reset and counts are made for the correct number of TIX (TOGGLE IN TRANSFER), RNW (READ NEXT WORD), RS (READ STROBE), and EOT's (END OF TRANSFER).

V. DETAILED TEST DESCRIPTION (continued)

3.0 Read Order Test, No-Chaining (continued)

Next the maintenance card is operated in the Fast Mode. This mode overrides the service request delay to force continuous service requests when required. The test description of the preceding paragraph will be repeated in this mode with the addition of a complete check of the IOAW being performed and the transfer of a 2K word block being timed. It should be noted that while operating in the fast mode, the CPU may be locked out of memory during data transfers.

The RETURN RESIDUE order is also tested in this section utilizing the Device End option set in the control word. Both the Immediate Device End (IDE) bit and the Terminate on Test Count (TTC) bit are exercised. Using the device end bits all residue bits are checked high and low.

The steps in this section are numbered from 220 to 247 and are executed by setting the Section Select Switch 3.

4.0 Write Order Test, No-Chaining

The Write Order test is almost identical to the Read Order test. Differences in this test involve checking the OUT XFER (out transfer) bit in the status word and counting the TOX (toggle out transfers) and WS (write strobes). The IOAW is not checked here and the writes consist of various segments of the 4K block read in the previous section. If the previous section was not executed, then the program will initialize the block.

The steps in this section are numbered from 250 to 277 and are executed by setting the Section Select Switch 4.

5.0 Read Order Test, Chained

Several groups of chained READ orders are exercised in this section and checked for data input in correct order, no gaps between blocks, and the correct number of TIX's, EOT's, RNW's and RD STRBS. In addition, the order prefetch function of the selector channel will be tested. These checks will be performed in both the fast and slow service request modes.

The steps in this section are numbered from 300 to 317 and are executed by setting the Section Select Switch 5.

V. DETAILED TEST DESCRIPTION (continued)

6.0 Write Order Test, Chained

This section tests the chained WRITE order. Checks are made to insure that the data is in the proper order and that the correct number of TOX's, EOT's, and WT STRBS occur. Order prefetch is also checked and all tests are performed in both fast and slow service request modes.

The steps in this section are numbered from 320 to 337 and are executed by setting the Section Select Switch 6.

7.0 Error Response Test

Various programmed error responses are checked in this section. The selector channel responses tested are to different device numbers, Service Out (SO) timeout, Service Request (SR) timeout, and illegal SIO orders. The device number test (executed over selector channel only) programs the maintenance card to respond with its data buffer instead of the hardwired device number at the initiation of an SIO program.

The steps in this section are numbered from 340 to 367 and are executed by setting the Section Select Switch 7.