26067A/B SYSTEM INTERFACE
OPTION 003

SERIAL INTERFACE

(FOR HP 256X LINE PRINTERS)

PART NUMBER 26067-90903

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GENERAL INFORMATION

1-1. INTRODUCTION

This manual provides general information, installation, theory, and service information for the Hewlett-Packard 26067A serial interface (part no. 5061-1707).

This section includes a general description and specifications for the interface.

1-2. GENERAL DESCRIPTION

The serial interface (5061-1707) enables a user to operate an HP 2563/65/66A Line Printer on a serial communications line using RS-232-C protocol (on a system which supports the specific printer). This interface provides point to point serial communications for full duplex asynchronous data transfer.

The interface is designed to receive data at one of seven baud rates (300, 600, 1200, 2400, 4800, 9600, and 19,200) and can be configured for any of the various data stream protocol handshakes or hardware handshakes (refer to paragraph 2-4, Interface Configuration).

The serial interface consists of a single printed circuit assembly (PCA), part number 5061-1707, which is installed into the printer backplane interface connector. The interface is available either as a factory installed option (opt 049) or as a kit for field installation. The HP 26067A Serial Interface Kit provides the Serial Interface PCA (5061-1707) for field installation. The kit also includes this manual (part no. 26067-90901).

The interface connector is a standard RS-232 style, 25-pin, D-subminature socket type connector. (The RS-232 signals used by the interface are listed in table 4-5.)

1-3. SPECIFICATIONS

The serial interface is designed for operation in the HP 256X Line Printer. Therefore the interface electrical specifications conform to the printer specifications. Printer specifications are provided in the HP 2563A Printer Operator's Manual (part no. 02563-90901) or the HP 2565/66A Printer Operator's Manual (part no. 02566-90901).

General specifications for the interface are listed in table 1-1.

TABLE 1-1. SPECIFICATIONS

* * * * * Electrical Characteristics * * * * *
POWER REQUIRED: +12 Volts +/- 5% @ 50 mA max. -12 Volts +/- 5% @ 50 mA max. + 5 Volts +/- 5% @ 1500 mA max. All power is supplied by the printer through the backplane connector to the interface PCA.
* * * * * Mechanical Characteristics * * * * *
SIZE: 20 cm (7.87 in.) by 27.7 cm (10.9 in.)
* * * * * Environmental Specifications * * * * *
OPERATING TEMP: 0 to 55 Degrees C (32 to 131 Degrees F)
OPERATING SURVIVAL: -20 to 65 Degrees C (-29 to 149 Degrees F)
RELATIVE HUMIDITY: 10% to 90% @ 40 Degrees C

SECTION II. INSTALLATION AND CONFIGURATION

2-1. INTRODUCTION

This section provides unpacking information, installation instructions, and configuration information for the serial interface (part no. 5061-1707).

2-2. UNPACKING AND INSPECTION

Before unpacking, inspect the shipping container for signs of mishandling. If damage to the shipping carton is evident, write a notation on the freight bill before signing. The package should be inspected as soon as possible.

After unpacking, check the interface and accessories for damage (cracks, broken parts, etc.). If the interface and/or accessories are damaged or fail to meet the published specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately for a carrier's inspection report.

Retain the shipping container and the packing materials for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-3. INTERFACE INSTALLATION

Installation of the interface into the printer (see figure 2-1) consists of removing/opening the printer top cover/panel, inserting the interface into the printer backplane interface connector, and finally configuring the interface for system operation.

WARNING

Since the installation of the interface requires the removal of the printer's protective covers, it is to be installed by a qualified Hewlett-Packard service representative.

Removal of the printer's protective covers by unqualified persons may result in serious personal injury.

Installation of the interface is described in the following steps (a #1 posidrive screwdriver is required):

a. Disconnect power to the printer by setting the Main Power switch, at the back of the printer to OFF (0).

b. Remove/open the printer cover/panel to gain access to the printer interface connector as directed in the appropriate 256X line printer service manual (part no. 02563-90904 / 02566-90904).

c. Disconnect the I/O cable from the existing interface and remove the interface from the printer. In the HP 2565/66A printers, two screws must be removed from the interface connector shield which sceures it to the frame; and, in the HP 2563A printers, a ground wire must be disconnected.

d. Insert the new interface into the backplane interface connector (the connector towards the rear of the printer), making certain that the interface is scrurely seated.

e. Ground the interface to the printer:

   HP 2563A Printer - Connect the I/O ground wire (from the printer) to the interface ground lug (see figure 2-1).

   HP 2565/66A Printer - Secure the interface PCA connector shield to the printer frame using the two screws removed in step c.

f. Replace/close the printer cover/panel.

g. Connect the system I/O cable to the printer interface connector.

h. Apply power to the printer by setting the Main Power Switch to ON (1).

i. Configure the interface (refer to paragraph 2-4, interface configuration, for configuration information).

j. Run the internal I/O self-test (refer to paragraph 4-4) to verify the operation of the interface. (The printer self-test, performed by pressing the TEST key, does not perform the I/O self-tests, to run the I/O self-tests they must be selected and run as a subtest from the operator control panel.)

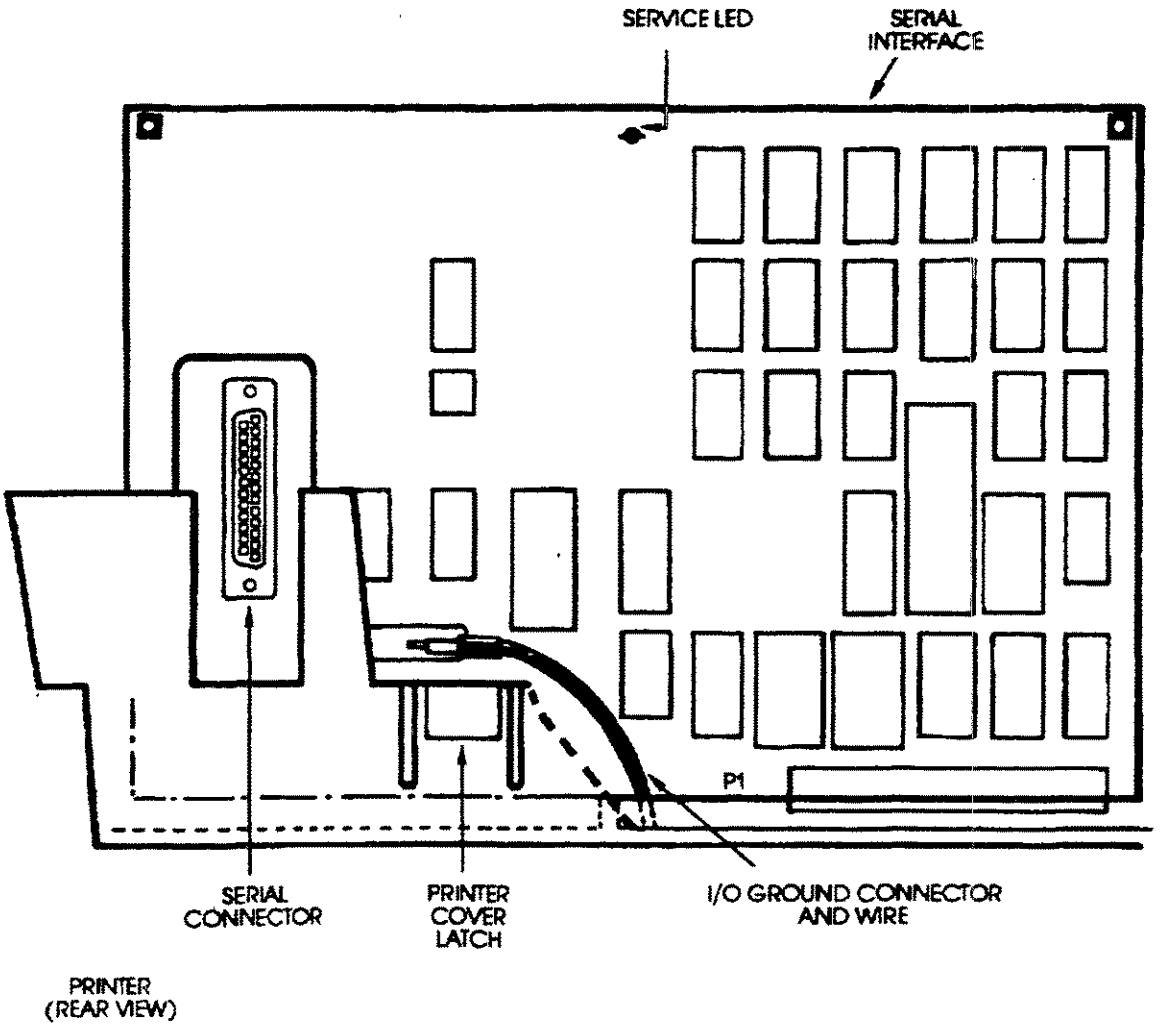


Figure 2-1. HP 2563A Printer Interface Installation

2-4. INTERFACE CONFIGURATION

For the interface to communicate with the system, the interface must be configured to the system configuration. Configuration of the interface is accomplished by selecting and entering function and configuration numbers into the Operator Control Panel with the interface installed in the printer and power applied. Function and configuration numbers are entered into the 256X printer Operator Control Panel in the same manner as other printer functions (refer to the 256X Operator's Manual for printer configuration information). The interface uses four configuration bytes to configure the interface. The four configuration numbers are selected by means of the four function numbers (20, 21, 22, and 23) (The 256X printer provides function numbers 20 through 29 for interface configuration but the serial interface only requires four configuration bytes for configuration.)

Each configuration byte identifies a group of functions for configuration. The configuration number for function number 22, for example, configures the display "1" on the printer Operator Control Panel for inactive CF or CC RS-232 signal, and baud rate functions. The parameter values for each function are selected in the configuration byte by selecting the proper bit values. Figure 2-3 identifies the bit locations for the configuration byte functions for each of the four function numbers. Detailed descriptions for the function parameters bit values are described in paragraph 2-6.

The configuration byte associated with each function number is an eight-bit binary number where the value of the bits determine the function parameters (see figure 2-3). To configure the interface for the system, select the function parameter bit (1 or 0) which matches the system configuration and set the bits as required for the configuration byte.

After the function parameter bit values have been determined for the byte, The byte is entered into the printer Operator Control panel. To enter the byte into the Operator Control Panel, the byte must be converted into a hexadecimal number for the printer. Convert the eight-bit binary number into a hexadecimal number and enter it into the printer. Figure 2-2 illustrates an example of a configuration byte conversion from the binary byte to the two-digit hexadecimal number.

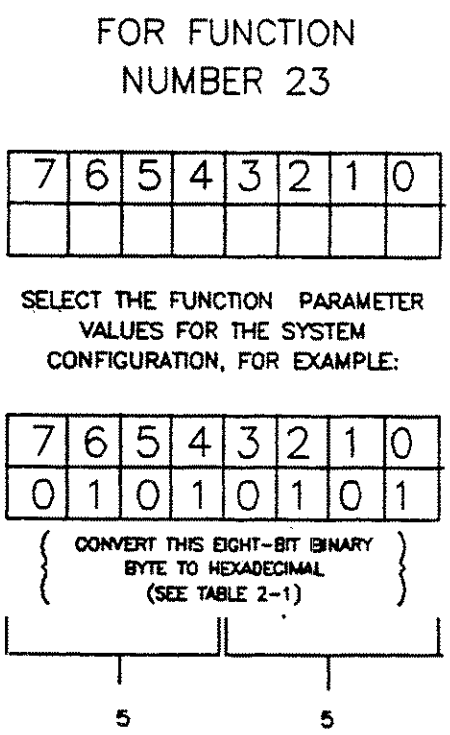


Figure 2-2. Example For Deriving Configuration Number

TABLE 2-1. BINARY TO HEXADECIMAL NUMBER CONVERSION

BINARY	HEX	BINARY	HEX
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

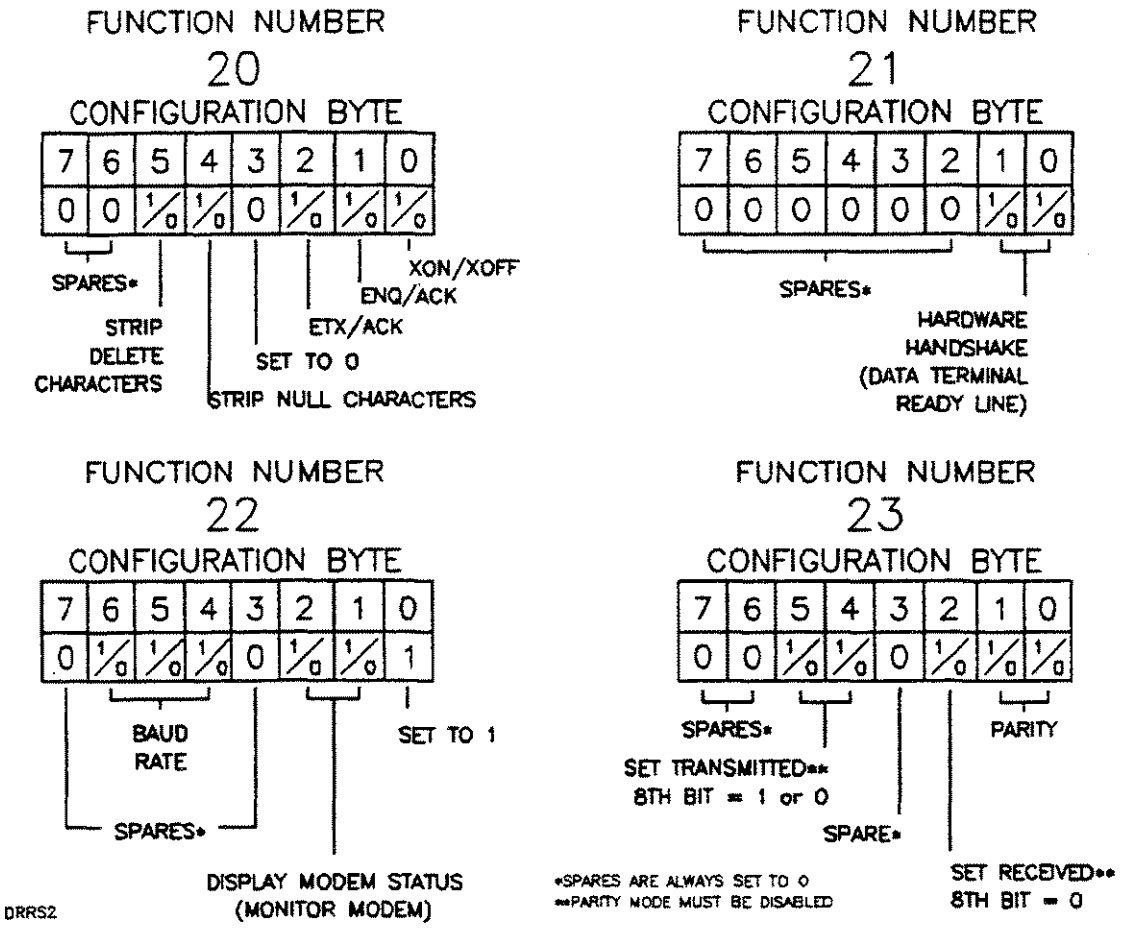


Figure 2-3. Configuration Bytes

2-5. OPERATOR CONTROL PANEL INTERFACE CONFIGURATION

The serial interface is configured using the 256XA printer Operator Control Panel. To configure the interface for the desired function parameters, perform the following steps:

a. Press the [ON LINE] key on the Operator Control Panel to take the printer off-line (if the printer is on-line). Power should be applied to the printer.

b. Press and hold the [CONFIG] key on the Operator Control Panel. This action displays the function number in the Operator Control Panel display.

c. Select the desired function number (20, 21, or 23) on the Operator Control

Panel display by pressing either the FINE ADJ. key (to increment the displayed number) or the ▼ key (to decrement the displayed number).

d. Release the CONFIG key. Releasing the CONFIG key displays the configuration number.

e. Select the configuration number (refer to paragraph 2-2, Interface Configuration) on the Operator Control Panel display by pressing either the FINE ADJ key (to increment the displayed number) or the ▼ key (to decrement the displayed number).

f. Press the ENTER key. This finalizes the configuration procedure and returns the printer to normal operation (the printer operating status of "0" should be displayed to indicate normal operation). If the key is not pressed the above configuration selections are not saved.

NOTE

If the CONFIG. key is pressed instead of the ENTER key the previous configuration is retained and the just-entered configuration value is discarded.

g. Return to step b. to configure the next function number (until all function numbers, 20, 21, 22 and 23, have been configured).

2-6. FUNCTION PARAMETER DESCRIPTIONS

Descriptions of the function parameters for function numbers 20, 21, 22 and 23 are provided below.

a. Function Number 20

Function number 20 configures the interface for the type of data stream handshake protocol (XON/XOFF, ENQ/ACK, or ETX/ACK) and for the removal of null and delete characters from the data stream.

The data stream handshake may be used by the system to prevent possible loss of data transmitted to the serial interface. When the interface data buffer is full (has reached its upper limit) and is unable to store any more data the

interface is considered busy. In the busy condition the interface can not accept data from the computer and must indicate to the computer that it is busy by using one of three data stream handshake protocols. (or the hardware handshake). Only one of the data stream handshakes can be used.

1. XON/XOFF (Bit 0)

   When bit 0 is set to 1, XON/XOFF handshake protocol is enabled by the interface. With XON/XOFF the interface will send an XON (DC1; 11 HEX) when it goes to the not busy condition and XOFF (DC3; 13 HEX) when it goes into the busy condition.

   When bit 0 is set to 0, XON/XOFF handshake is disabled.

2. ENQ/ACK (Bit 1)

   When bit 1 is set to 1, Enquiry(ENQ)/Acknowledge(ACK) handshake protocol is used. With ENQ/ACK handshake protocol the ASCII enquiry character (05 Hex) is sent to the interface by the computer before the computer sends a data block of characters. If the interface is busy it will not respond until it goes out of the busy condition, at which point it will sent the Acknowledge character (06 Hex) to inform the computer to send a 256-byte data block.

   When bit 0 is set to 0, ENQ/ACK handshake is disabled.

3. ETX/ACK (Bit 2)

   Bit 2 when set to 1, ETX/ACK handshake protocol is enabled. The ETX/ACK protocol is functionally the same as the ENQ/ACK protocol with the exception that the ENQ character is replaced with the ETX (03 Hex) character.

   When bit 2 is set to 0, ETX/ACK handshake is disabled.

4. Strip Null Characters (Bit 4)

   If bit 4 is set to 1, null characters (00 or 80 Hex) are stripped (removed) from the data stream by the interface; if bit 4 is set to 0 this feature is disabled and no action is taken on the null characters.

   Nulls are sometimes used for timing delays or other purposes and may be placed anywhere in the data stream. When the printer is in display functions mode, null characters will not be printed if null stripping is enabled.

5. Strip Delete Characters (Bit 5)

If bit 5 is set to 1, delete characters (7F or FF Hex) are stripped (removed) from the data stream; if bit 4 is set to 0 this feature is disabled and no action is taken on the delete characters.

Deletes may be used for timing delays or other purposes and may be placed anywhere in the data stream. When the printer is in display functions, delete characters will not be printed if delete stripping is enabled.

b. Function Number 21

Function number 21 configures the interface for hardware handshake protocol.

The hardware handshake uses the Data Terminal Ready (CD) RS-232 signal line to indicate the interface busy condition. This mode of operation can be used if the printer is connected directly to the computer or another device (such as a terminal) and not to a modem.

The interface provides four ways of using the CD line to indicate interface busy/not busy condition. Bit 0 and bit 1 can be configured to enable the CD line for normal RS-232 operation, handshake busy operation, handshake inverted busy, or on-line/off-line operation (shown in table 2-2) as described below.

To select the desired function parameter, insert the parameter bits as shown in table 2-2.

TABLE 2-2. HARDWARE HANDSHAKE SELECTION

BITS 1 0	DESCRIPTION
0 0	Normal operation
0 1	CD line busy operation
1 0	CD Line Inverted Busy Operation
1 1	On-Line/Off-Line Operation

1. Normal Operation (Bit 0 & 1)

When both bit 0 and bit 1 are set to 0, the CD line is used for normal RS-232 operation of this line (for use with a modem or data set). (The line will be held high.)

2. Hardware CD Line Busy Operation (Bits 0 & 1)

When bit 0 is set to 1 and bit 1 is set to 0 the interface uses the CD line to indicate busy/not busy operation. When the interface is busy the CD line will be high and when the interface is not busy and can accept data, the CD line will be low.

3. Hardware CD Line Inverted Busy Operation (Bits 0 & 1)

When bit 0 is set to 0 and bit 1 is set to 1 the interface uses the CD line to indicate busy/not busy operation. When the interface is busy the CD line will be low and when the interface is not busy and can accept data, the CD line will be high.

4. On-Line/Off-Line Operation (Bits 0 & 1)

When both bit 0 and bit 1 are set to 1 the CD line indicates on-line/off-line condition of the printer. When the CD line is high, the printer is on-line and when the CD line is low, the printer is off-line.

a. Function Number 22

Function number 22 configures the interface for display "1" (modem status) for active CC or CF signal and baud rate. These functions are described below.

1. Bit 0 always set to 1

2. Display Modem Status (Bits 1 & 2)

If the Display Modem Status function is enabled, then, when the Data Set Ready (CC) signal or the Carrier Detect (CF) signal becomes inactive, the printer operating status on the Operator Control Panel will switch from "0" to "1". When the signal becomes active again the printer status will return to "0". Only one signal line, either the CC or CF, can be selected at a time for the Display Mode Status mode. The bits used to enable this feature are listed in table 2-3, below.

TABLE 2-3. DISPLAY "0" FOR INACTIVE CC OR CF SIGNAL

BITS 2 1	DESCRIPTION
0 0	Disable Display Modem Status
0 1	Display "0" when the CC signal is active.
1 1	Display "0" when the CF signal is active.
1 0	Not Used, invalid selection

3. Baud Rate (Bits 4, 5, and 6)

Bits 4, 5, and 6 select the baud rate at which the interface operates. Table 2-4 lists the parameter values for the indicated baud rates.

TABLE 2-4. BAUD RATE SELECTION

Bit 6	Bit 5	Bit 4	Baud Rate
0	0	0	300
0	0	1	600
0	1	0	1200
0	1	1	2400
1	0	0	4800
1	0	1	9600
1	1	0	19200

d. Function Number 23

Function number 23 configures the interface for parity and for the selection of the received and/or transmitted eighth-bit to either 1 or 0.

1. Parity (Bit 0 & 1)

Bits 0 and 1 select the type of parity used by the interface. Parity can be selected for no parity, even, or odd parity. The bit values for these parity parameters are shown in table 2-5, below.

TABLE 2-5. PARITY SELECTION

BITS 1 0	DESCRIPTION
0 0	Disable parity
0 1	Enable even parity
1 1	Enable odd parity
1 0	Not Used;

2. Set Received 8th-Data Bit to 1 (Bit 2)

The interface can set the eighth-bit of each received data byte to 0. If bit 2 is set to 1, the interface sets the 8th-bit of each received data byte to 0; if bit 2 is set to 0, the 8th-bit is left as received.

The parity function must be disabled to set the received 8th-bit to 1.

3. Set Transmitted 8th-Data Bit to 1 or 0 (Bits 4 & 5)

The interface can set the 8th-bit of each transmitted byte to either a 1 or a 0, or transmit the byte unchanged. Table 2-6 identifies the bit settings for the 8th-bit selections.

The parity function must be disabled to set the transmitted 8th-bit to either 1 or 0.

TABLE 2-6. TRANSMITTED 8TH-BIT SELECTION

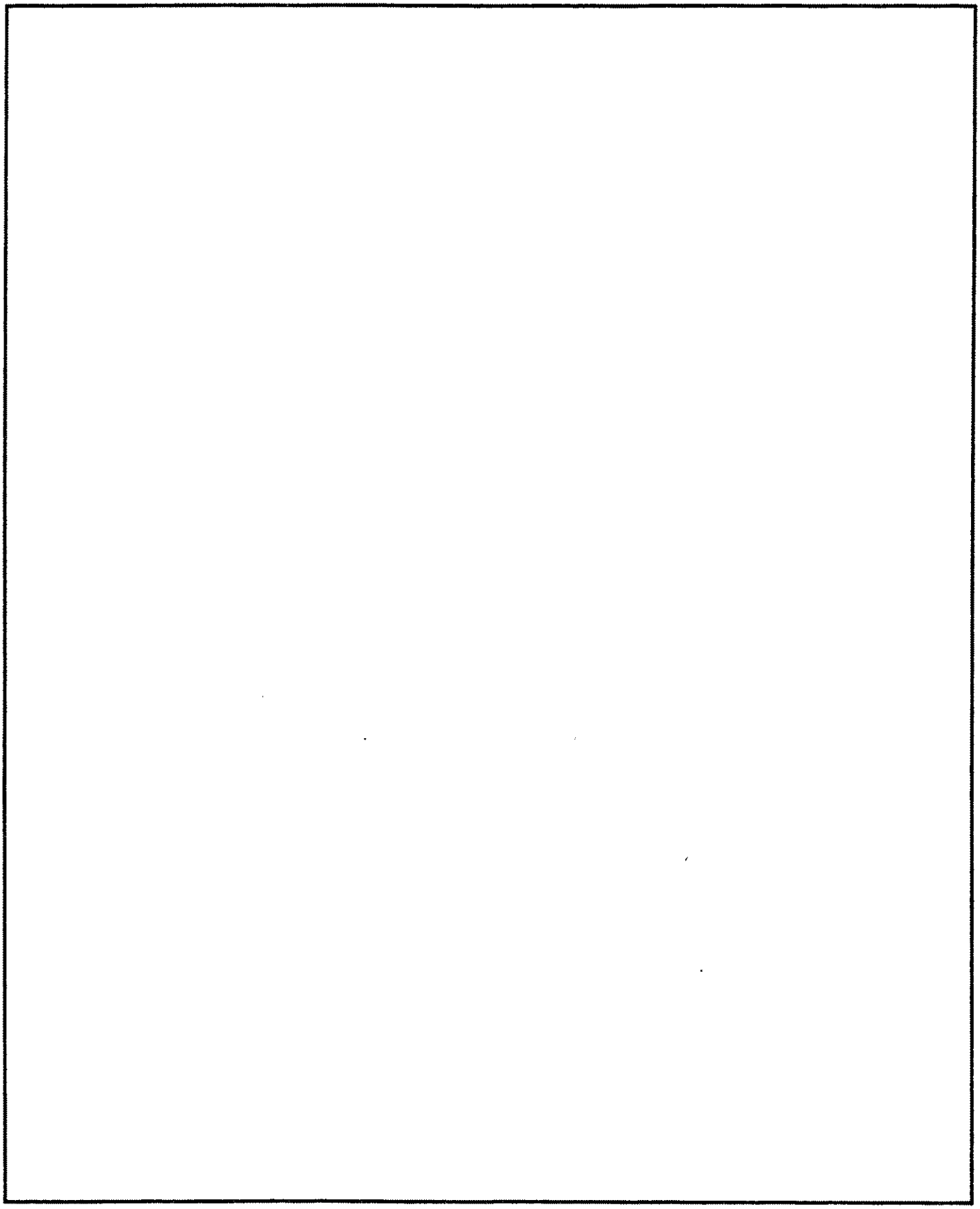
BITS 5 4	DESCRIPTION
0 0	TRANSMIT 8TH-BIT AS IS
0 1	SET TRANSMITTED 8TH-BIT = 0
1 0	SET TRANSMITTED 8TH-BIT = 1
1 1	INVALID SETTING; NOT USED

2-7. TYPICAL CONFIGURATION

A typical configuration for the serial interface when operating the 256X printer as a spooled printer on an HP 3000 system will generally look as shown below.

FUNCTION NUMBER	CONFIGURATION BYTE	
20	31	- Nulls and Deletes stripped, XON/XOFF protocol
21	00	- Normal Data Terminal Line operation (always = on)
22	51	- 9600 Baud Rate, CTS Signal line Ignored, Modem Status disabled
23	03	- Odd Parity

To verify the interface configuration values run the printer self-test (press the [TEST] key and then the [ENTER] key). The print-out generated by the self-test includes a listing of the interface configuration.



SECTION III.
THEORY OF OPERATION

3-1. INTRODUCTION

This section provides the theory of operation for the serial interface. A brief description of the printer/interface communication protocol is provided, followed by a description of the serial interface circuitry. The serial interface circuits are described on a functional level (see figure 4-4) to provide a general understanding of the operation of the interface.

3-2. MASTER/SLAVE SHARED MEMORY COMMUNICATION PROTOCOL

The printer control electronics and the interface electronics communicate with each other through the "shared" I/O RAM memory located on the serial interface (see figure 3-1). When either the printer or the interface electronics has information to transfer to the other (interface or printer), the information is stored into the I/O RAM, by either the printer or the interface initiating the command, and removed by the other (interface or printer). That is, if the interface has information for the printer, the interface stores the information into the I/O RAM memory and the printer reads the information from the I/O RAM memory. Thus, both printer and interface share this memory for information exchange. This shared memory communication protocol identifies the printer as the master and the interface as the slave.

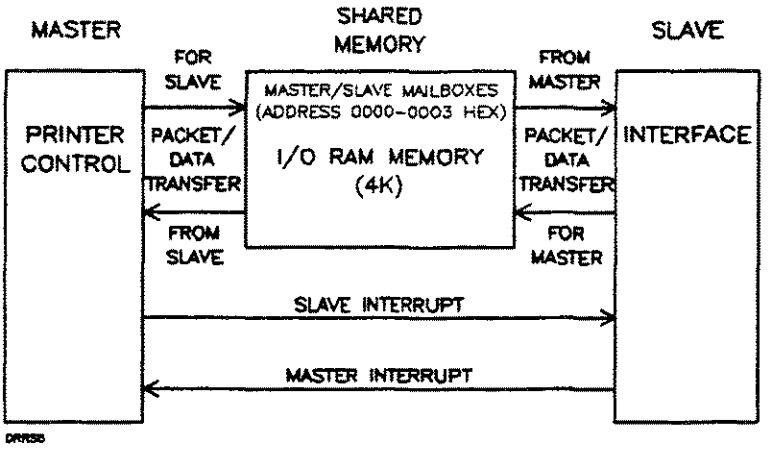


Figure 3-1. Master/Slave Shared Memory Communication Protocol

The master/slave shared memory communication protocol uses a format referred to as a packet to implement this protocol. The packet (see figure 3-2) is created by the originator (master or slave that requires the other perform a command) of the command and contains all the information required to inform the receiver (master or slave) of the command as to the command operation it is requested to perform. These operations include the transfer of print data from the slave to the master, self-test information transfer between the master and slave, printer configuration data transfer from the master to the slave, or status information transfer from the slave to the master.

The packet, created by either the master or slave, consists of a block of 18 bytes of data. Each byte of the packet contains information that the originator of the packet needs to pass to the receiver of the packet, who performs the requested command operation. The packet includes a Command byte and a Command Modifier byte which identify the command that the packet originator needs performed. A Return Command Status byte to indicate to the packet originator the status of the packet command execution. The return command status byte is read by the originator of the packet when the originator retrieves the packet after being interrupted by the the receiver after the command execution. Also, if any data, such as data to be printed, is associated with the command, the packet Buffer Address byte identifies the beginning I/O RAM memory address where this data is stored and the Data Length byte identifies the number of bytes stored. A buffer type and length bytes are also included in the packet as required by the system operation to identify the type and size of the I/O sharred memory location that is being used.

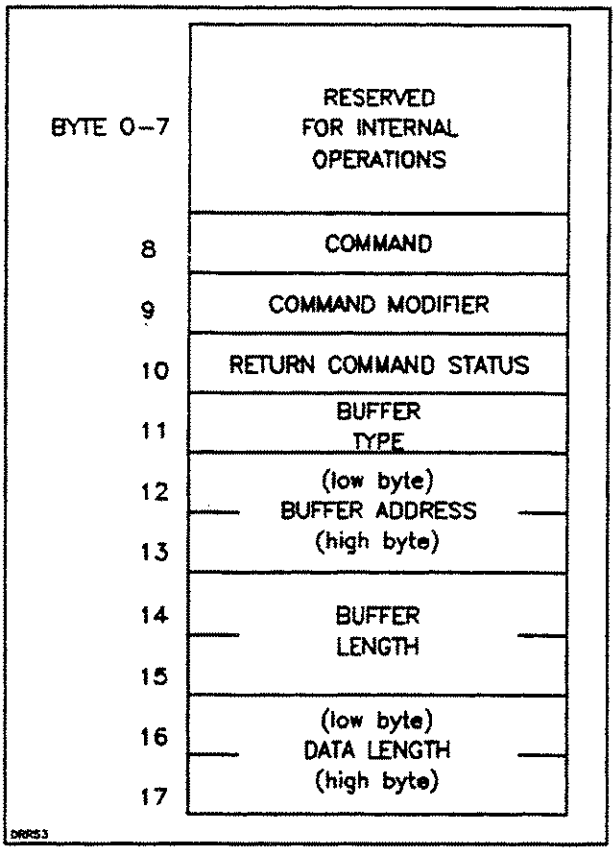


Figure 3-2. Packet Format

The first four I/O RAM memory locations (0000 Hex -0003 Hex; see figure 3-3) are reserved for the originator of a packet to indicate to the other that an operation needs to be performed. The master places its requests for the slave into the first two locations of memory (0000 Hex and 0001 Hex; referred to as the slave's mailbox) and the slave places its requests for the master into the second two memory locations (0002 Hex and 0003 Hex; referred to as the master's mailbox). These two bytes identify the beginning I/O RAM memory address location of the the packet. Thus, if the master has a command for the slave, the master will place the two packet address bytes into the first two locations of memory (0000 and 0001 Hexadecimal) and then interrupt the slave. The master interrupts the slave by means of the Slave Interrupt (INTSLV) signal line. This interrupt prompts the slave to read its I/O RAM mailbox memory locations to obtain the address of the packet.

When either the master or the slave has a command and/or data to transfer to the other, the originator (master or slave initiating the command) creates a packet for

the command information and transfers the packet to the I/O RAM memory. Also, any data associated with the command is transferred into I/O RAM memory. Then the originator places the memory address of the packet into the receivers (master or slave performing the command) mailbox and interrupts the receiver. The receiver retrieves the address of the packet from its mailbox. Once the receiver has the address of the packet, the receiver retrieves the packet and performs the operation. When the receiver of the packet has completed the packet operation (or is unable to complete the command or gets unexpected results), the receiver writes the status into the packet Returned Command Status byte (byte 10), returns the packet into the shared memory, and interrupts (hardware interrupt) the originator. The interrupt prompts the originator to look for a packet address in its mailbox, retrieve the packet, and read the status. This sequence allows the master and slave a means of transferring information to each other, through the shared memory.

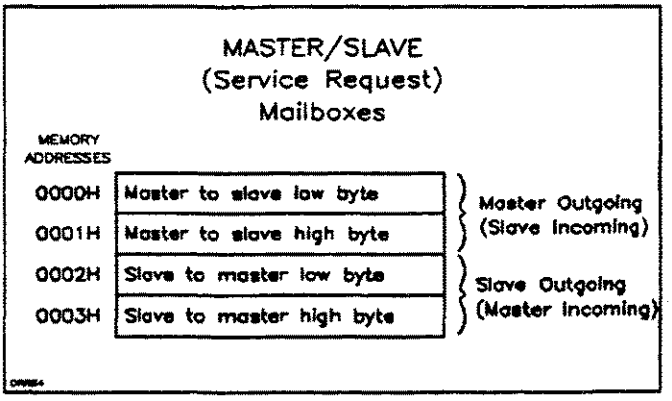


Figure 3-3. Master/Slave Request Format

3-3. FUNCTIONAL CIRCUIT DESCRIPTION

The serial interface (see figure 4-4) transfers data to the printer from the computer and status information from the printer to the computer. This information exchange is accomplished across the serial RS-232-C data communication line. The interface circuits are described below on a functional level, followed by a description of data flow through the interface.

3-4. FUNCTIONAL CIRCUITS

The interface circuitry consists of control electronics and memory circuits. The memory includes 4K of read only memory (ROM) and 4K of I/O random access memory (I/O RAM). The control electronics consists of the I/O processor, the serial control circuits and the I/O control circuitry (see figure 4-4).

a. I/O Processor

The I/O processor (a Z80 microprocessor) provides the main control for interface operations, which include interpreting and executing commands, writing data into the I/O RAM memory, and generation and regulation of packet information for the master. It provides control signals to the I/O control circuitry and the serial control circuits, across the I/O processor control lines and address bus. These control signals are generated by the I/O processor through the operation of the I/O operating program contained in the I/O ROM. The I/O operating program provides the necessary information for the I/O processor to determine the proper action to be taken.

b. I/O Control Circuitry

The I/O control circuitry receives input control signals from the I/O processor and from the printer control processor control lines and address buses. The I/O control circuitry controls access to the I/O RAM memory by the master or I/O slave circuits. Since the I/O RAM memory is shared by both the master and I/O slave and only one may access the memory at a time, the control circuitry regulates which processor (master or slave) is allowed to access the memory. This includes control of the Address Multiplexer for selection of either the master or slave address bus used for addressing the I/O RAM memory and control of the bi-directional bus gates to allow the master data bus or the I/O slave data bus access to the I/O RAM. The control circuitry controls the Address Multiplexer by means of the Address Select ($\overline{AS}$) signal. Whichever processor is selected to read or write into or from the I/O RAM memory, its address bus is selected for addressing. The I/O RAM memory access is provided to the processors on a first-come-first-serve basis.

The bi-directional bus gates divide the data bus into separate sections, to allow either the master or slave processor data bus use of the shared I/O RAM memory. These gates are normally disabled and must be enabled by the control circuitry to allow data to pass.

c. Serial Control Circuitry

The serial control circuitry regulates all serial communications operations involved in the transfer of data/command information to and from a Datacomm modem (data set) or a directly connected computer or other device. The serial circuitry includes the serial input/output (SIO) circuit, the counter timer chip (CTC), the Normal/Loopback Data circuits and signal line drivers and receivers. The SIO circuit converts incoming serial data from the data line into eight-bit parallel data for the interface bus and converts outgoing eight-bit parallel data into serial data as required for serial data transmission. The SIO also uses the baud rate clock received from the counter timer chip for timing operations for receiving and transmitting data.

The CTC provides the internal Baud Rate Clock signal for the SIO. The CTC uses a 615.38 KHz clock, which is the 8 MHz clock divided by 13, to generate the required baud rate clock. The frequency of the baud rate clock generated by the CTC is determined by configuration bytes received by the CTC across the data bus from the I/O processor. These bytes issued by the I/O processor configure the CTC for the required baud rate clock frequency. The I/O processor uses the operator input configuration information to determine the baud rate clock.

In the normal mode the Normal/Loopback Data Select circuitry allows data on the Data In and Data Out lines to the SIO to pass normally into and out of the interface, but when the loopback mode is enabled, data from the Data Out line is directed back into the SIO through the input data line for testing.

3-5. CIRCUIT OPERATION

A brief description of the data flow through the interface is used to provide a general understanding of how the various interface circuits work together to transfer data. This description describes a data transfer from the system controller, through the serial interface to the printer control circuits.

When the computer has data for the printer, the computer sends the data to the printer and the SIO circuit begins receiving the serial data from the interface line receivers. The SIO, which maintains a status byte to indicate that it has received a data byte, updates the status byte when it receives a byte.

When the SIO receives a byte it interrupts the I/O processor. The I/O processor reads the SIO status and if the status indicates that the SIO contains a data byte, the SIO contains a data byte, the I/O processor will transfer the data byte.

To transfer a data byte from the SIO circuitry to the I/O processor, the I/O processor directs the SIO to output the byte onto the bus and the I/O processor reads the data byte. If the byte is a handshake byte for the I/O processor it will be used by the processor and eventually discarded; if the byte is data it must be transferred into the I/O RAM memory.

Print data is stored into the shared I/O RAM using the master/slave shared memory communication protocol (described in paragraph 3-2). This requires that the I/O processor create a packet for the printer control processor identifying the command and the amount and location of data involved and then store this packet data into the I/O RAM.

For the I/O processor to write a data byte into the I/O RAM memory, the I/O processor enables $\overline{\text{MREQ}}$ and $\overline{\text{WR}}$. When these lines to the control circuitry are enabled, the control circuitry determines if the I/O RAM memory is available (is not being accessed by the printer control processor). Since the I/O RAM memory is

shared by the printer control processor and the I/O processor, only one processor may access the memory at a time. If the printer control processor is using the I/O RAM memory, the I/O processor may be required to wait. If the I/O RAM memory is not available the control circuitry will generate WAIT signals which hold off the I/O processor from accessing the I/O RAM memory until it becomes available. When the I/O RAM memory becomes available the WAIT signal is discontinued and the I/O processor is given access to the I/O RAM to allow the data transfer.

When the I/O processor is given access to the I/O RAM the control circuitry enables the Address Select (AS) signal to the address multiplexer to select the I/O processor address lines for addressing the I/O RAM and it also enables the Bi-Directional Bus gate B to allow data from the I/O processor to pass to the I/O RAM memory. To enable the Bi-Directional Bus gate for a I/O processor write to the I/O RAM memory, the I/O control circuitry generates the Gate (GATE) signal and the Direction (DIR) signal to enable the Bi-Directional Bus gate B for the transfer. The GATE signal enables the gate and the DIR signal selects the direction data is allowed to pass through the gate.

Each byte is transferred from the SIO across the bus into the I/O processor. The I/O processor addresses a location in the I/O RAM and the Control Circuitry Address Select line enables the Address Multiplexer to pass the I/O processor addresses to the I/O RAM. The I/O processor addresses and places the data byte onto the bus. The I/O RAM memory will store the byte when the Write Enable (WE) signal from the control circuitry becomes active. The I/O processor transfers the byte back onto the data bus into the I/O RAM. For each byte the I/O processor selects an I/O RAM address, outputs the address across the address bus and writes the data into the I/O RAM memory at that location.

Each byte of data received by the SIO is transferred into memory in this manner until all the data is transferred. When the final byte of data is written into the I/O RAM memory, the I/O processor will complete the packet information and write it into the packet memory location.

When the data transfer operation is complete the I/O processor will interrupt the printer control processor to let it know that the interface shared I/O RAM contains information for the printer.

The I/O processor interrupts the printer control processor by enabling the Interrupt Master (INTMAS) signal. Since any one of several slaves can enable the INTMAS signal line, the printer control processor must poll the slaves to identify the one requiring service. To identify the interrupting slave the printer control processor enables the Interrupt Acknowledge (INTACK) signal line. This line is common to all slave circuits. Any slave which interrupted the printer control processor will resopnd to the INTACK by enabling its Poll Acknowledge (POLACK) signal line. Each slave circuit has its own unique POLACK signal line which is used by the printer control processor to identify the source of an interrupt. Since the I/O slave requires service, it will enable its POLACK line . When the printer control processor is ready to accept data from the interface, it will respond to the interrupt request by the interface.

For the printer control processor to communicate with the interface the printer control processor must access the I/O RAM and retrieve the information (packet and data) placed there by the I/O processor. For the printer processor to address the I/O RAM, it must gain access to the I/O RAM in the same manner as the I/O processor. The printer control processor enables its Memory Request ($\overline{\text{MEMREQ}}$) and Read ($\overline{\text{RD}}$) signals to the I/O control circuitry. If the I/O processor is not using the I/O RAM for any operation, the I/O control circuitry allows the printer control processor access to the I/O RAM. The I/O control circuitry enables the Bi-Directional Bus Gate A allowing the printer control processor data bus access to the I/O RAM and the control circuitry also enables the Address Select signal to the address multiplexer to allow the master address bus addresses to access the I/O RAM memory.

Thus the data from the system controller is passed through the serial interface to the printer. The transfer of data from the printer to the system controller through the interface is identical except the direction is reversed.

SECTION IV. MAINTENANCE

4-1. INTRODUCTION

This section provides troubleshooting information and parts replacement information for the serial interface.

4-2. TROUBLESHOOTING

Troubleshooting the interface PCA in the HP 256X line printer is similar to HP terminals. When a problem occurs, define the problem, its frequency (whether intermittent or redundant), and the length of time the problem has been occurring. (It may be possible to correlate the onset of the problem with an event such as updating the system software or adding new hardware.)

To begin troubleshooting perform the printer I/O subtests for the interface to check both the interface and the cabling. Also observe the service LED located on the interface. This LED can be used to evaluate the operation of the interface (refer to paragraph 4-3).

4-3. I/O LED

When the printer is powered-up or reset it performs a power-up check sequence. During this sequence the printer initiates the interface internal I/O self-test (subtest 31) and, after the completion of the test, the interface communicates the results of the test to the printer processor. If the interface completes the internal self-test satisfactorily and communicates the results to the printer as required, the I/O LED will flash at a 1/2 Hz rate. If the interface passes its internal test but cannot communicate with the printer processor, the I/O LED will flash at a 5 Hz rate. This 5 Hz flash indicates that an error exists and this error is most likely something other than the interface (although it may be the interface). If the interface performs the communication satisfactorily but fails the internal I/O subtest the LED will remain either continuously on or off.

TABLE 4-1. SERVICE LED ERROR INDICATIONS

LED	ERROR DESCRIPTION
1/2 Hz FLASH	Interface operating correctly.
5 Hz FLASH	Passed I/O subtest but failed to communicate with printer processor (Printer or possibily the interface).
ON or OFF STEADY	Interface failed subtest (I/O RAM, ROM, or SIO/CTC circuitry failure likely).

4-4. I/O SELF-TEST DIAGNOSTIC

The I/O self-test diagnostic is resident in the interface I/O RAM memory and consists of three sections or subtests: the internal test (test number 31), the modem loopback test (test number 32), and the 25-pin loopback test (test number 33). To run these I/O self-tests each one must be selected and executed from the HP 256X printer Operator Control Panel as a printer subtest.

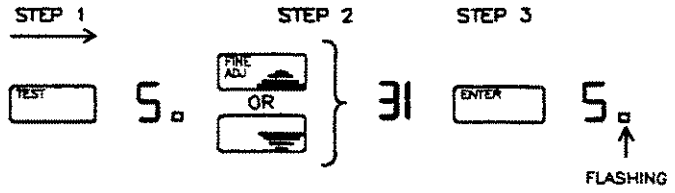
NOTE

The printer self-test (initiated by pressing the [TEST] key on the operator panel) does not execute the I/O self-test diagnostic. The I/O subtest must be individually selected and executed from the operator control panel.

If an I/O subtest is initiated and completes satisfactorily the printer displays the printer-ready status (0 is displayed in the operator display panel); if an error is detected the printer display flashes 50. The printer error code 50 indicates an interface error. Additional information as to the nature of the error can be obtained by pressing the [ENTER] key on the operator panel. Pressing the [ENTER] key displays the fail code number in the display. Fail codes, listed in table 4-2, identify the specific interface circuitry which has failed.

To run an I/O subtest for a single test execution or continuous (looping) execution, perform the following steps:

* To run a single serial I/O subtest:



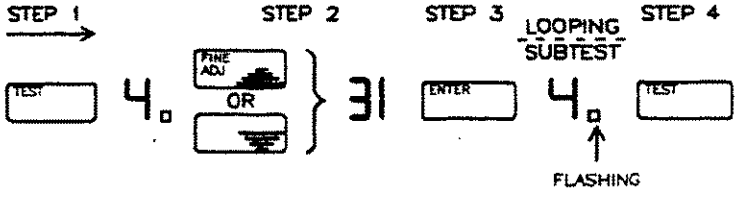
STEPS

1 - Press and hold the TEST key (less than 1 sec.) until a five appears in the Operator Control Panel display (when the TEST key is released the displayed 5 will switch back to 0).

2 - Select the serial I/O subtest number (31, 32, or 33) in the printer Operator Control Panel display.

3 - Press the ENTER key to run the subtest.

* To run the serial I/O subtest continuously (loop on test):



STEPS

1 - Press and hold the TEST key (approximately 5 sec) until a four appears in the Operator Control Panel display (a 5 will appear first and then switch to a four, then when the TEST key is released the 4 will switch back to a 0).

2 - Select the serial I/O subtest number (31, 32, or 33) in the printer Operator Control Panel display.

3 - Press the ENTER key to run the subtest.

4 - press the TEST key to terminate the continuous subtest.

TABLE 4-2. I/O SELF TEST FAIL CODES

ERROR NUMBER	ERROR DESCRIPTION
00	NO ERRORS DETECTED
01	RAM ERROR
02	ROM ERROR
03	SIO/CTC CIRCUITRY ERROR
04	MULTIPLE FAILURES

4-5. SUBTEST 31 (INTERNAL I/O)

The internal I/O subtest performs three routines which check the I/O RAM, I/O ROM, and SIO/CTC circuitry. If any one of these tests fail, a fail code can be accessed to identify which routine failed. If any two, or all three of the routines fail, a multiple-error fail code is provided. These fail codes for the subtest routines are listed in table 4-2.

After the internal subtest has completed, If no errors are detected, a zero is displayed in the printer Operator Control Panel. If an error is detected the printer I/O error number 50 will flash in the printer display.

If the interface passes subtest 31, subtest 32 can be run, with the 25-pin loopback connector (part no. 02620-60062) connected directly to the interface connector to check the output control lines on the interface which are not checked by subtest 31.

4-6. SUBTEST 32 (MODEM LOOPBACK)

Loopback test 32 allows the user to test control and data signal paths between the interface and a modem. The following signal lines are tested:

Transmitted Data to Received Data
Ready-To-Send to Clear-To-Send
(others as required for modem operation)

The modem loopback test can be performed either with the local or remote modem (see figure 4-1) placed in the loopback test mode.

a. THE LOCAL MODEM IS PUT IN THE DATA LOOPBACK TEST MODE (if the local modem has the capability for data loopback). Refer to the modem manual for instructions on how to place the modem into data loopback test mode. Once the local modem is set to loopback test mode, initiate the modem loopback test (self-test 32) from the printer Operator Control Panel of the HP 256X line printer.

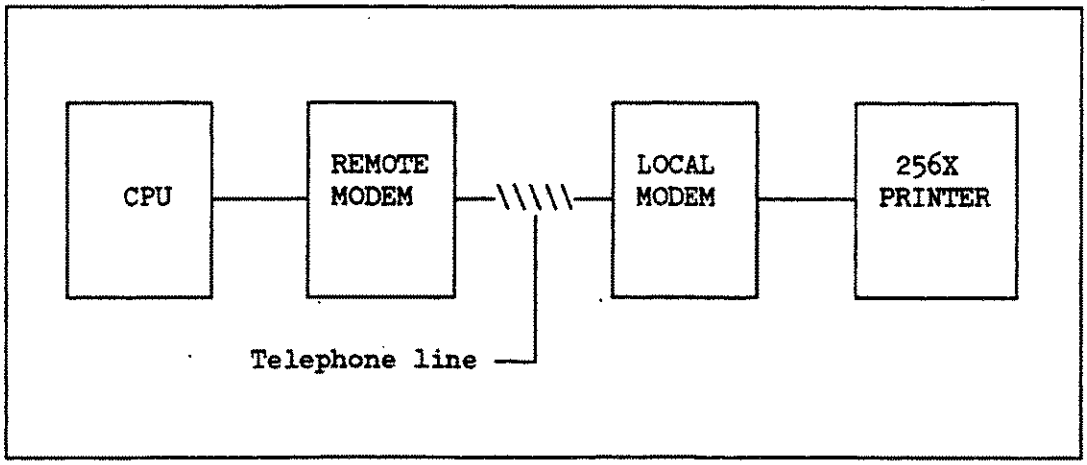


Figure 4-1. Modem Loopback Test 32

b. THE REMOTE MODEM IS PUT IN THE DATA LOOPBACK TEST MODE (if the remote modem is able to loopback data sent from the local modem). Refer to the modem manual for instructions on how to place the modem into data loopback test mode. Once the remote modem is set to loopback test mode, initiate the modem loopback test (subtest 32) from the printer Operator Control Panel of the HP 256X line printer.

After the loopback test 32 is completed a zero is displayed in the Operator Control Panel display if no error was detected. If an error was detected the I/O error code (50) will appear, flashing, in the panel display. (A fail code of 3 will always be presented for a modem loopback test failure.)

A modem loopback test failure indicates that the interface, the cables, or a modem may have failed. The 25 pin loopback test should be run to determine if the interface has failed.

4-7. SUBTEST 33 (25-PIN LOOPBACK)

Test 33 allows the user to test the control and data signals in the signal path between the serial interface and the point where the loopback is accomplished. A 25-pin loopback connector (part no. 02620-60062), required for this test, is plugged into the CPU end of the serial I/O cable. This connector physically loops the output signal lines to the input signal lines.

The signal lines checked by self-test 33 are listed below:

Transmit Data	to	Receive Data
RTS	to	CTS and Carrier Detect
DTR	to	DSR

This test is initiated from the Operator Control Panel of the HP 256X line printer. This test checks the I/O control lines and then transmits its entire character set at the configured baud rate.

If the test completes and no errors were detected, a zero will appear in the panel display. If an error is detected, testing will stop and the I/O error code (50) will appear, flashing, in the panel display. (A fail code of 3 is always presented for a 25-pin loopback test failure.)

NOTE

The 25-pin loopback plug (02620-60062) can be connected directly to the 25-pin connector on the back of the printer to test the control and data signal path on the interface PCA.

4-8. REPLACEMENT PARTS AND DIAGRAMS

The replacement parts, diagrams, and schematics are provided in tables and figures on the following pages.

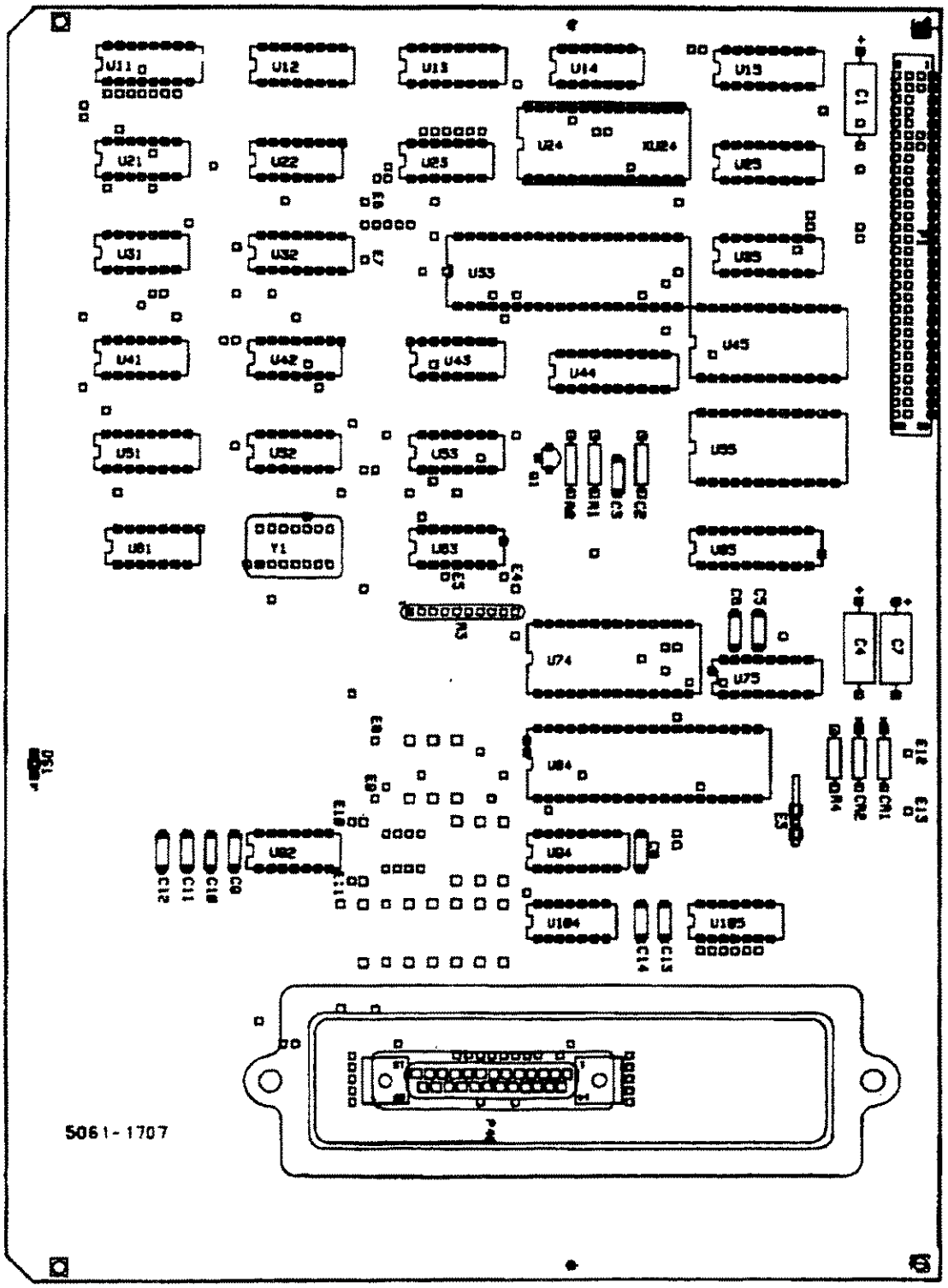


Figure 4-2. Serial Interface PCA (5061-1707), Parts Location

TABLE 4-3. SERIAL INTERFACE PCA (5061-1707) PARTS LIST

REF. DES./ INDEX NO.	DESCRIPTION	PART NO.
C1,4,7	CAP:F 6.8UF TANT 35V	0180-0116
C2	CAP:F 33PF 5% 100V	0160-4807
C3,5,6	CAP:F 0.01UF 20% DIP	0160-5298
C8-14	CAP:F 330 PF 5%	0160-5311
CR1,2	DIO:SW 1N4150	1901-1098
DS1	LED	1990-0671
P1	CONN:POST-TP-SKT	1251-7308
P40	CONN:25 PIN F	1251-4946
Q1	XSTR:PNP 2N3906	1853-0036
R1	RES:F 33K 5% .25W	0683-3335
R2	RES:F 22 5% .25W	0683-2205
R3	RES:PACK 9-2.2K 2% .125W	1810-0277
R4	RES:F 4.7K 5% .25W	0683-4725
U11,32	IC:SN74LS279N	1820-1440
U12,13	IC:SN74LS138N	1820-1216
U14	SN74S03N GATE	1820-0682
U15,25,35	IC:SN74LS298N	1820-1444
U21,22	IC:SN74LSOON	1820-1197
U23	IC:SN74LS32N	1820-1208
U24	PROM SERIAL I/O	5061-1710
U31	IC:SN74LS02N	1820-1144
U33	IC:Z80A-CPU-PS	1820-2298
U41,61,105	IC:SN74LS14N	1820-1416
U42,52,63	IC:SN74S74N	1820-0693
U43	IC:SN72LS51N	1820-1210
U44,65	IC:SN74LS245N	1820-2075
U45,55	IC:HM6116P-3	1818-1611
U51	IC:SN74LS175	1820-1195
U53	IC:SN74LS126AN	1820-1645
U74	IC:Z80A-CTC-PS	1820-2301
U75	IC:SN74LS161N	1820-1430
U84	IC:Z80A-SIO/PO	1820-2518
U92	IC:MC1489AL	1820-0990
U94	IC:SN74LS153N	1820-1244
U104	IC:SN74S03N	1820-0682
XU24	SCKT: 28 PIN IC	1200-0567
Y1	CLK OSC 8MHz	1813-0188

TABLE 4-4. INTERFACE BACKPLANE CONNECTOR (P10) SIGNAL CONNECTIONS

PIN	SIGNAL	PIN	SIGNAL
1	+5	2	+5
3	+5	4	+5
5	[-TURNAROUND]	6	NOT USED
7	+12	8	+12
9	-12		-12
11	GND	12	GND
13	GND	14	GND
15	[TCLOCK]	16	[-MLOAD]
17	[POSITION STRB]	18	[-NMI]
19	[DATA OUT]	20	[-LOAD]
21	[-IOREQS]	22	[-MEMREQS]
23	-RESET	24	-INT
25	[CLOCK 7 to 8 MHz]	26	-WAIT
27	-READ	28	-WRITE
29	A0	30	A1
31	A2	32	A3
33	A4	34	A5
35	A6	36	A7
37	A8	38	A9
39	A10	40	A11
41	A12	42	A13
43	A14	44	A15
45	S0	46	S1
47	S2	48	S3
49	D0	50	D1
51	D2	52	D3
53	D4	54	D5
55	D6	56	D7
57	-INTACK	58	-POLACK (See Note)
59	-IOREQSL (See Note)	60	-MEMREQSL (See Note)

Note: Pins 58,59,60 are slot dependent signals.

TABLE 4-5. INTERFACE CABLE CONNECTOR (P40) SIGNAL CONNECTIONS

PIN	SIGNAL
1	AA (Frame Ground)
2	BA (Transmit Data)
3	BB (Receive Data)
4	CA (Request-To-Send)
5	CB (Clear-To-Send)
6	CC (Data-Set-Ready)
7	AB (Signal Ground)
8	CF (Carrier Detect)
20	CD (Data Terminal Ready)