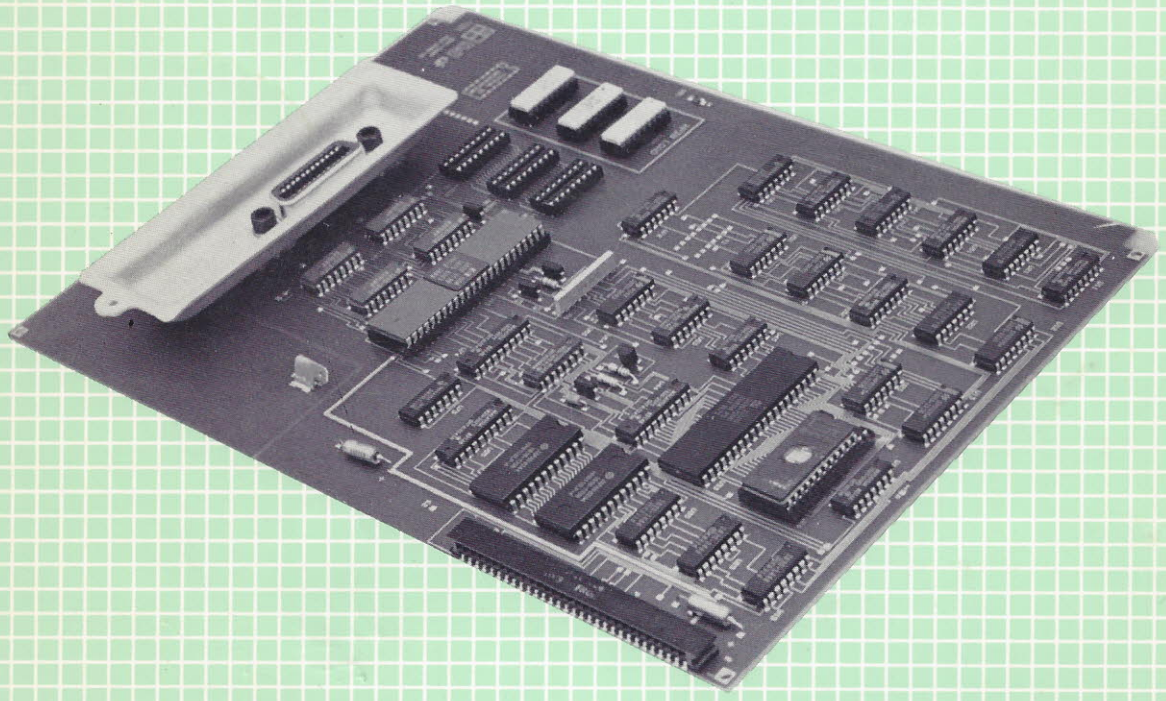
26067A/B

HEWLETT PACKARD

HPIB INTERFACE



26067B SYSTEM INTERFACE
OPTION 001

HP-IB INTERFACE

(FOR 256X LINE PRINTERS)

PART NUMBER 26067-90901

HEWLETT PACKARD

Publication History

Changes in text to document updates subsequent to the initial release are supplied in manual update notices and/or complete revisions to the manual. The history of any changes to this edition of the manual is given below. The last update itemized reflects the machine configuration documented in the manual.

Any changed pages supplied in an update package are identified by an update number adjacent to the page number. Changed information is specifically identified by a vertical line (revision bar) on the outer margin of the page.

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NOTICE

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Section I
General Information

1-1. INTRODUCTION

This manual provides general information, installation, theory, and service information for the Hewlett-Packard HP-IB Interface (part number 5062-0477).

This section includes a general description and specifications for the interface.

1-2. GENERAL DESCRIPTION

The HP-IB Interface (5062-0477) enables a user to operate an HP 256X Line Printer on the Hewlett-Packard Interface Bus (HP-IB).

The HP-IB interface consists of a single printed circuit assembly (PCA) part number 5062-0477 which is installed into the printer backplane I/O connector. The interface is available either as the factory installed standard printer interface or as a kit for field installation. The 26067B HP-IB Interface Kit provides the HP-IB Interface PCA (5062-0477) for field installation. The kit also includes this manual (part number 26067-90901) and a 4 metre cable.

The HP-IB Interface is designed for operation in the HP 256X Line Printer; thus, the interface electrical specifications conform to the printer specifications. Printer specifications are provided in the 256X Printer Operator's Manuals (part numbers 02563-90901, 02564-90901 and 02566-90901).

General specifications for the interface are listed in table 1-1.

TABLE 1-1. SPECIFICATIONS

***Electrical Characteristics**

POWER REQUIRED: +12 Volts +/- 5% @ 50 ma max. + 5 Volts +/- 5% @ 1500 ma max.

All power is supplied by the printer through the backplane connector to the interface PCA.

***Mechanical Characteristics**

SIZE: 13.8cm (5.4 in.) by 27.3 cm (10.8 in.)

***Environmental Specifications**

OPERATING TEMP: 0 to 55 Degrees C (32 to 131 Degrees F)

RELATIVE HUMIDITY: 10% to 90% @ 40 Degrees C

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Section II.
Installation and Configuration

2-1. INTRODUCTION

This section of the manual describes how to install the HP-IB Interface (5062-0477) into the printer, how to adjust HP-IB cable loading, and how to configure the HP-IB interface functions for the system. It also covers unpacking and inspection of the HP 26067B System Interface kit.

2-2. UNPACKING AND INSPECTION

If the shipping container is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office (these offices are listed at the back of this manual.)

Retain the shipping container and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit.

2-3. INTERFACE INSTALLATION

Installation of the interface into the printer consists of removing/opening the printer cover/panel, adjusting the HP-IB loading, inserting the interface into the printer backplane interface connector, and configuring the interface. Installation of the interface is described in the following steps.

WARNING

Any operation which requires the removal of the printer's protective covers must be performed by a qualified Hewlett-Packard service representative. Unqualified personel may contact voltage points in the printer causing serious personal injury or death.

a. Set the Main Power On/Off switch at the back of the printer to off (0).

b. Remove the printer cover/panel as directed in the appropriate printer service manual.

c. Adjust the HP-IB loads on the interface as required for the total system cable length (see paragraph 2-6, Cable-I/O Cable Loading).

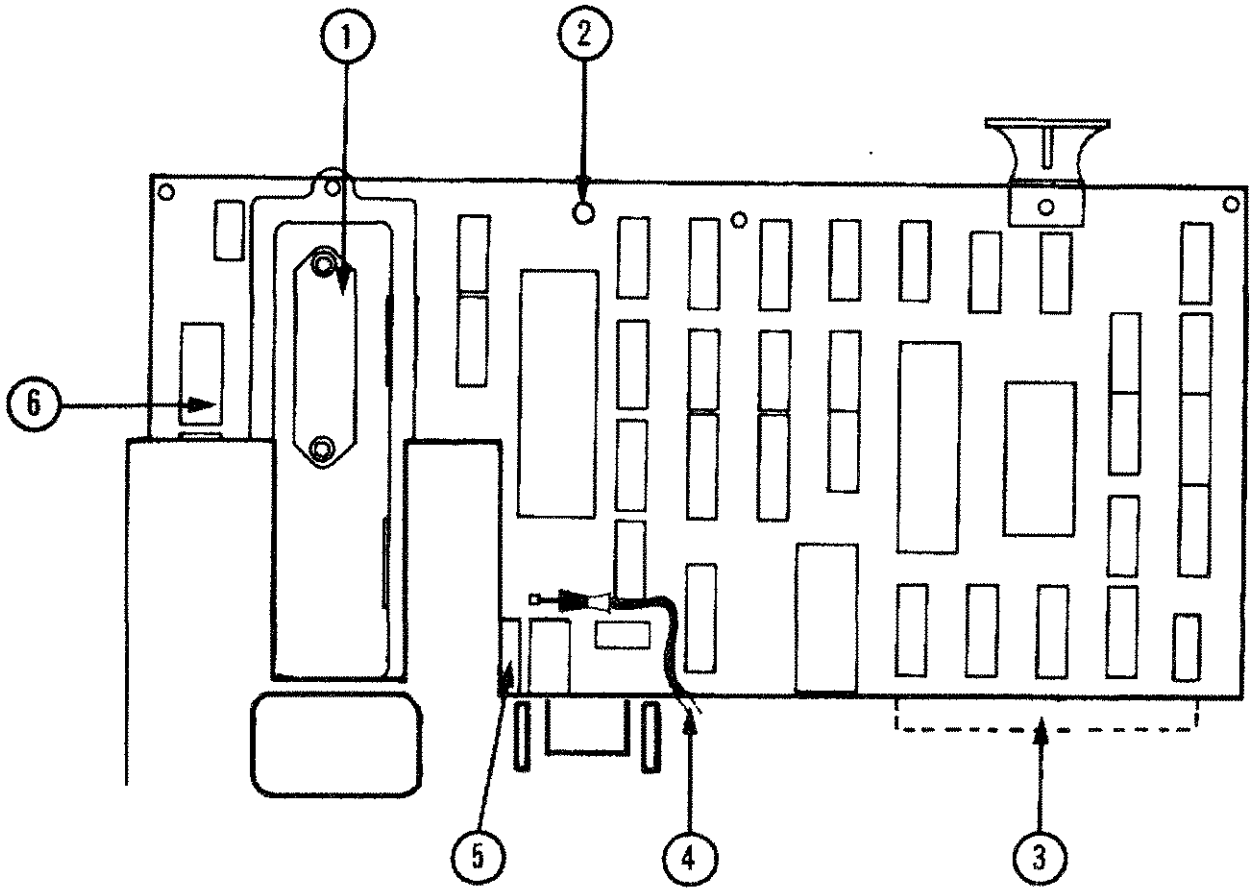
d. Insert the HP-IB Interface PCA into the rear (I/O) printer slot.

e. Connect the printer ground wire from the printer Backplane/Analog PCA to the HP-IB interface PCA (see figure 2-1).

f. If the printer is being installed and requires configuration and the configuration requires CE mode (see paragraph 2-5), for convenience install the CE jumper mode in this step.

NOTE

The non-CE functions can be configured when the printer is in the CE mode.



1. HPIB Connector
2. Service LED
3. I/O Connector
4. HPIB Ground
5. HPIB Load Storage Sockets (3)
6. HPIB Load Sockets (3)

Figure 2-1. Interface Installation

g. Replace/close the printer top cover/panel, but do not secure it.

h. Set the printer POWER switch to on (1).

i. Configure (or check) the CE mode functions and configuration settings on the printer Operator Control Panel (see paragraph 2-5, CE Mode Configuration).

j. Disconnect the power to the printer by setting the Main Power On/OFF switch at the back of the printer to off (0).

k. Lift the printer top cover from the printer and remove the CE mode jumper.

l. Replace and secure the printer cover.

m. Connect the HP-IB cable to the printer I/O connector (see figure 2-1).

n. Apply power to the printer.

o. Run self-test to verify operation of the interface (refer to paragraph 4-2, Self-Test).

2-4. HPIB ADDRESS CONFIGURATION

To configure the HP-IB printer/interface for operation requires that an HP-IB address be selected for the printer. The HP-IB address is configured in the same way that the other 256X printer features (print density, margins, etc.) are selected. To select an HP-IB address, select function number 20 and then enter an address (parameter) of 0 through 7.

To configure the HP-IB address, perform the following steps:

a. Press the [ON LINE] key to take the printer off-line (if the printer is on-line), power should be applied to the printer.

b. Press and hold the [CONFIG.] key on the Operator Control Panel. This action displays the function number in the Operator Control Panel display.

c. Select function number 20 on the Operator Control Panel display by pressing either the [FINE ADJ.] key (to increment the the displayed number up) or the [ ] key (to increment the number down).

d. Release the [CONFIG.] key. Releasing the [CONFIG.] displays the HP-IB address (parameter) number in the display.

e. Select the desired address 0-7 in the display in the same manner that the function number was selected in step c, using the [FINE ADJ.] and [ ] keys.

f. Press the [ENTER] key. This finalizes the configuration and returns the printer to normal operation. If the [ENTER] key is not pressed the above configuration selections are not saved.

2-5. PROTOCAL CONFIGURATION

There are 3 HP-IB configurations for the HPIB Interface. The configurations are as follows:

CIPER (Function 25 = 0)

This is used for 1000(A/E/F/M),
3000(3X/4X/6X/7X), 9000(SRM),
9000(500 series direct) and
9845B/C(SRM).

BLOCK (Function 25 = 1)

This is used for 250/260 and the 64000 systems.

CHARACTER (Function 26 = 19)
(Function 27 = 83)
(Function 25 = 2)

This mode is used for 9000.
(200 series direct connect)

Character mode has no recovery mechanisms and returns no status to the CPU. Therefore the console will NOT report paper out, or transmission problems. Functions 26 and 27 are used as a lock word and must be set before changing function 25 for character mode.

*HP2536A ONLY. All of these configuration parameters can be changed via the panel on printers with control board firmware date code 2418 and greater (use self test to verify the firmware date code on control board). The printers prior (before) to 2418 must be in CE mode to change configuration parameters.

2-6. CABLE - I/O DRIVER LOADING

WARNING

Any operation which requires the removal of the printer's protective covers must be performed by a qualified Hewlett-Packard service representative. Unqualified personel inside the printer may contact voltage points causing serious personal injury or death.

An HP-IB cable connected to the HP-IB interface presents a load to the HP-IB interface driver circuits. Different bus cable lengths present different loads to the bus devices. To eliminate possible data rate reduction or data loss which might occur as a result of mismatched loading between the HP-IB devices and the cable loading, the HP-IB Interface (5062-0477) I/O driver is designed with variable loading. This variable loading enables compensation of the HP-IB interface for changes in cable loading (length).

The interface loading is designed such that one load unit (1 load) compensates for one metre of cable. For a good loading match the HP-IB bus requires that the number of metres of cable should be less than or equal to the total number of system device loads. The equation below describes these loading requirements.

```
  TOTAL CABLE LENGTH
(in metres) ≤ # of System (GIC) Loads
            + # of Printer Loads
            + # of Loads Of All
                 Other Bus Devices
```

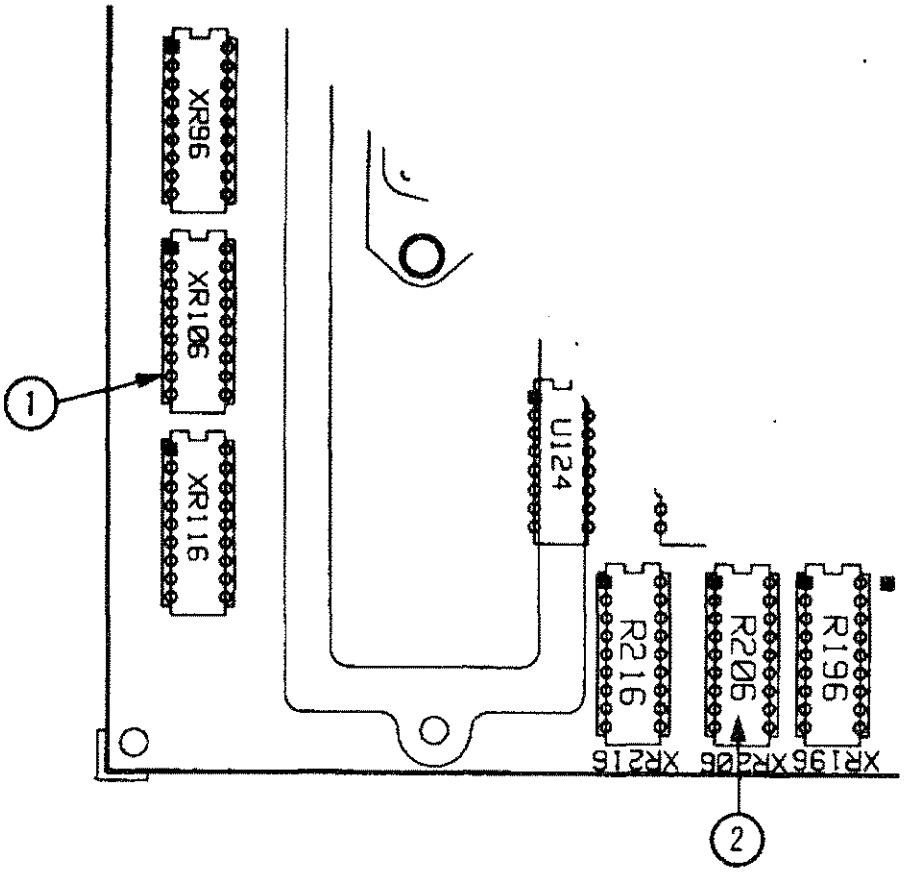
When calculating loading for a system, the number of loads (load units) in the system controller plus, all other bus devices must be added together to get the total number of I/O driver loads. The cable length is the total of all lengths (number of metres) of cable.

NOTE

When adding the number of metres of cable in a system, remember to include the internal cable in the bus devices if there is any.

The maximum number of loads is 15 for any bus, thus the maximum length of cable is 15 metres.

Bus devices are designed with a certain number of loads built into the circuit which are not removable. This type of load is referred to as an "internal" load where as the installable (removable) resistor pack loads are referred to as "installable" loads (or load packs). The HP-IB Interface I/O driver loading can be changed by inserting installable load packs (that contain either 1 load, 2 loads, or 4 loads) into the I/O driver load sockets (XR96, XR106, and XR116) on the interface PCA (see figure 2-2). One, two, or three load packs (that contain 1 load, 2 loads, and 4 loads), which are provided with the interface PCA, may be installed into the I/O driver circuitry load sockets. The total loading is the sum of the installed loads plus one (there is one internal load designed into the circuit which must also be added). This provides a variable



1. HPIB Load Storage Sockets (3 total)
   (Storage for load resistor packs when not in use)
2. I/O Driver Load Sockets (3 total)
   (For installed loads)

Figure 2-2. HP-IB Interface Load Locations

load range from 1 (1 internal design load; no installed loads) to 8 (three loads, "1 load", "2 load", and "3 load" installed plus the one internal design load). When the loads are not being used they are stored in storage sockets (XR96, XR106, AND XR116).

The HP-IB Interface (5062-0477) is shipped with 1 I/O load (1 internal design load and no load resistor packs installed).

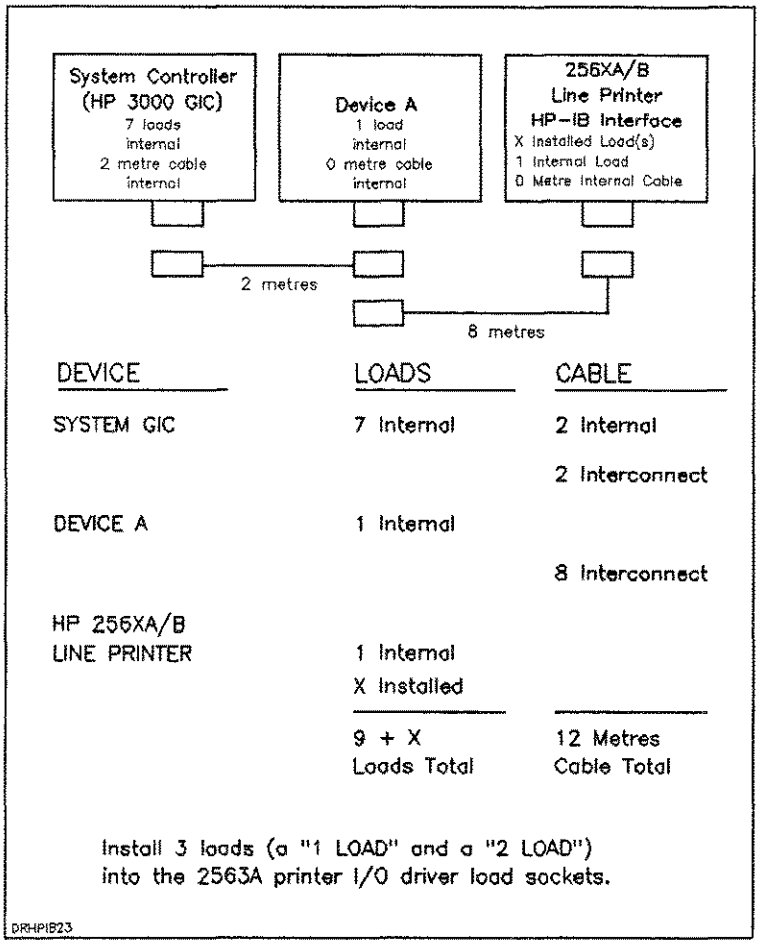


Figure 2-3. HP-IB Cable Loading Example

When installing or changing cabling, observe the following recommendations:

- Connect multiple devices to the system in a linear (serial/daisy-chain) configuration rather than in a star (radial/cluster) configuration.
- Connect the device containing the most loads furthest from the system controller.
- The maximum total cable length is 15 metres and total number of loads is 15 for any HP-IB bus configuration.
- The device containing the most internal loads should be connected with the longest cable.
- The total length of cable (in metres) used, must be less than or equal to the total number of device loads on the HP-IB bus.

If, For example, a system includes an HP3000, an HP 2563A Line Printer, and some other device (DEVICE A) as shown in figure 2-3, the loads are calculated as shown. For the number of loads to equal the number of metres of cable (12 metres), 3 loads need to be added since nine are already available. Thus, a 1 load and a 2 load resistor pack can be installed into the I/O driver load sockets, from the load storage sockets, to increase the number of total loads to 12.

SECTION III.
THEORY OF OPERATION

3-1. INTRODUCTION

This section provides the theory of operation for the HP-IB Interface. A brief description of the printer/interface communication protocol is provided, followed by a description the HP-IB interface. The HP-IB interface circuits are described on a functional level (see figure 3-1) to provide a general understanding of the operation of the interface.

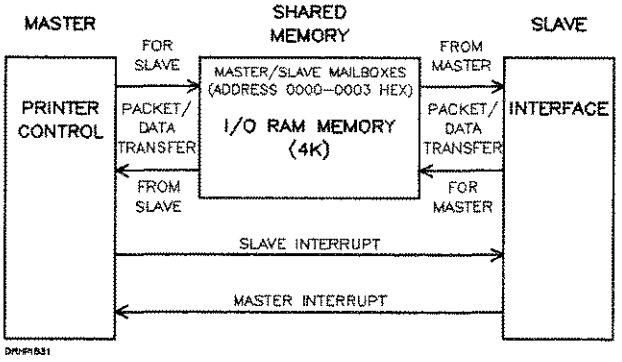


Figure 3-1. Master/Slave Shared Memory Communication Protocol

3-2. MASTER/SLAVE SHARED MEMORY COMMUNICATION PROTOCOL

The printer control electronics and the interface electronics communicate with each other through the "shared" I/O RAM memory located on the HP-IB interface (see figure 3-1). When either the printer or the interface electronics has information to transfer to the other (interface or printer), the information is stored into the I/O RAM, by either the master or the interface initiating the packet, and removed by the other (slave or printer). That is, if the interface has information for the printer, the interface stores the information into the I/O RAM memory and the printer reads the information from the I/O RAM memory. Thus, both printer and interface share this memory for information exchange. This shared memory communication protocol identifies the printer as the master and the interface as the slave.

The master/slave shared memory communication protocol uses a format referred to as a packet to implement the shared memory protocol. The packet (see figure 3-2) is created by the originator and contains all the information required to inform the master or slave as to what operation it is being requested to perform. These operations include the transfer of print data from the slave to the master for printing, self-test information transfer between the master and the slave, printer configuration data from the master to the slave, or status information transfer from the slave to the master.

The packet, created by either the master or slave, consists of a block of 18 bytes of memory. Each byte of the packet contains information that the originator (master or slave) of the packet needs to pass to the receiver (master or slave) of the packet. These commands might be print data command, self-test data exchange, or configuration information. The packet bytes include a Command byte and a Command Modifier byte which identifies the command the

packet originator needs performed. A Return Command Status byte to indicate Status byte is used to indicate to the packet originator the status of the command operation. Also, if any data, such as data to be printed, is associated with the command, the packet Buffer Address byte identifies the beginning I/O RAM memory address where this data is stored and the Data Length byte identifies the number of data bytes stored.

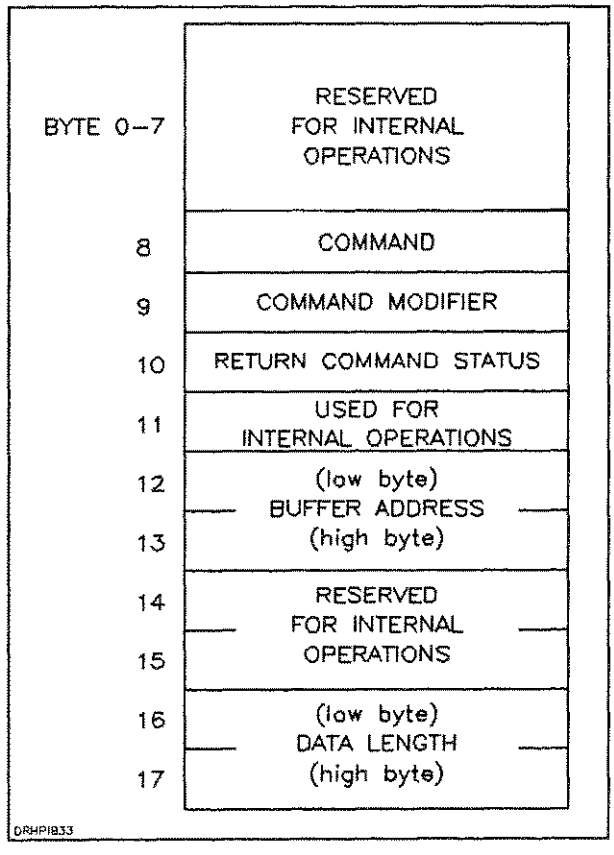


Figure 3-2. Packet Format

The first four I/O RAM memory locations (0000 Hex -0003 Hex; see figure 3-3) are reserved for originator (the master or slave) of a packet to indicate to the other (slave or master) that an operation needs to be performed. The master places its requests for the slave into the first two locations of the I/O RAM memory (0000 Hex and 0001 Hex; referred to as the slave's mailbox) and the slave places its requests for the master into the second two memory locations (0002 Hex and 0003 Hex; referred to as the master's mailbox). These two bytes identify the beginning I/O RAM memory address location where where the originator has placed the packet. Thus, if the master has a command for the slave, the master will place the two packet address bytes into the first two locations of memory (0000 and 0001 hexidecimal) and then interrupt the slave. The master interrupts the slave by means of the Slave Interrupt ($\overline{\text{INTSLV}}$) signal line. This interrupt prompts the slave to read its I/O RAM mailbox memory locations to obtain the address of the packet.

When either the master or the slave has a command and/or data to transfer for the other, the originator (master or slave initiating the command) must create a packet for the command information and transfers the packet to the I/O RAM memory. Also, any data associated with the command is transferred into memory. Then the originator places the memory address of the packet into the receivers (slave or master performing the command). The receiver retrieves the address of the packet from its mailbox. Once the receiver has the packet address, the receiver retrieves the packet and performs the operation. When the receiver of the packet has completed the packet operation (or is unable to complete the command or gets unexpected results), the receiver writes the status into the packet Returned Command Status byte (byte 10), returns the packet into the shared memory, and interrupts (hardware interrupt) the originator. The interrupt prompts the originator to look for a packet address in its mailbox, retrieve the packet, and read the status. This sequence allows the master and slave a means of transferring information to each other, through the shared memory.

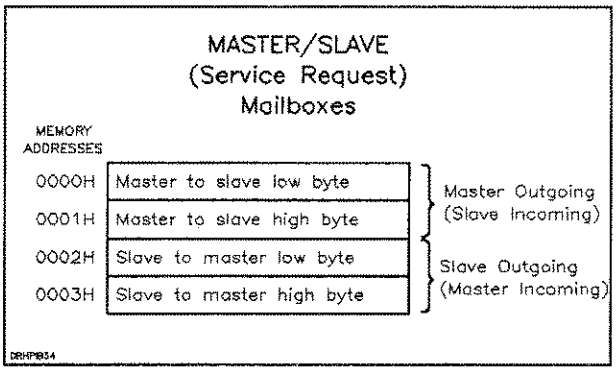


Figure 3-3. Master/Slave Request Format

3-3. FUNCTIONAL CIRCUIT DESCRIPTION

The HP-IB interface (see figure 4-4) transfers data to the printer from the computer and status information from the printer to the computer. This information exchange is accomplished across the Hewlett-Packard Interface Bus (HP-IB) using HP-IB protocol. The interface functional circuits are described below, followed by a functional circuit operation description.

3-4. FUNCTIONAL CIRCUITS

The interface circuitry consists of control electronics and memory circuits. The memory includes 8K of read only memory (ROM) and 4K of I/O random access memory (RAM). The control electronics consist of the I/O processor, the HP-IB processor and the I/O control circuitry.

a. I/O Processor

The I/O processor (a Z80 microprocessor) provides the main control for interface operations which includes interpreting and executing commands received from the printer processor and from across the bus, writing data into the I/O RAM memory, and generation and regulation of packet information for the master. It provides control signals to the I/O control circuitry and to the HP-IB processor. The I/O processor provides control through the operation of the I/O operating program contained in the I/O ROM.

b. I/O Control Circuitry

The I/O control circuitry receives input control signals from the I/O processor and from the printer control processor control lines and address buses. The I/O control circuitry controls access to the I/O RAM memory by the master or I/O slave circuits. Since the I/O RAM memory is shared by both the master and I/O slave and only one may access the memory at a time, the control circuitry regulates which processor (master or slave) is allowed to access the memory. This includes control of the address multiplexer for selection of either the master or slave address bus used for addressing the I/O RAM memory and control of the bi-directional bus gates to allow the master data bus or the I/O slave data bus access to the I/O RAM. The control circuitry controls the address multiplexer by means of the address select ($\overline{AS}$) signal. Whichever processor is selected to read or write into or from the I/O RAM memory, its address bus is selected for addressing. The I/O RAM memory access is provided to the processors on a first-come-first-serve basis.

The bi-directional bus gates divide the data bus into separate sections, to allow either the master or slave processor data bus use of the shared I/O RAM memory. Also, since the data bus is common through the printer, these gates separate the bus, allowing both processors to transfer data across their respective sections of the bus at the same time. These gates are normally disabled and must be enabled by the control circuitry to allow data to pass.

c. HP-IB Processor

The HP-IB processor manages all HP-IB bus protocol control operations involved in the transfer of data/command information to and from the HP-IB bus. Data or commands received on the HP-IB bus are transferred across the interface data bus to the I/O processor for action. Commands transferred across the HP-IB bus are handled by the I/O processor and the required action taken. The HP-IB processor performs these bus communications as directed by the I/O processor; and, the I/O processor as directed by the printer processor.

3-5. CIRCUIT OPERATION

A brief description of the data flow through the interface is used to provide a general understanding of how the various interface circuits work together to transfer data. This data flow describes the transfer of data from the computer to the HP-IB interface, where it is stored until the printer is ready to accept it.

The computer initiates the transfer when it has data for the printer by issuing an HP-IB Request To Write command to the interface When the HP-IB processor (see figure 4-4) receives the command from the bus it sets the End Or Secondary Interrupt (-EOSINT) signal which inturn sets the INT signal to the I/O processor. The I/O processor Interrupt (-INT) signal, when enabled, informs the I/O processor that some circuit requires action.

The I/O processor can be interrupted by any one of three interrupts: End Or Secondary Interrupt ($\overline{\text{EOSINT}}$), HP-IB Interrupt ($\overline{\text{HPIBINT}}$), or the Slave Interrupt ($\overline{\text{INTSLV}}$). The slave Interrupt signal is generated by the I/O control circuitry, when the printer processor requests access to the I/O RAM memory. The other two interrupt signals, EOSINT and HPIBINT, are generated by the HP-IB processor. The HPIBINT is enabled if the HP-IB processor receives an HP-IB Device Clear command across the bus or a parity error is detected on the bus. The EOSINT signal is enabled if an HP-IB command or the last data byte of a data block is received across the HP-IB bus. Since, in this case, the $\overline{\text{EOSINT}}$ interrupt enables the I/O processor will read the data/command from the HP-IB processor.

To transfer the command from the HP-IB processor to the I/O processor, the I/O processor will identify the action to the HP-IB processor through the address select lines and then enables the I/O Go ($\overline{\text{IOGO}}$) signal. I/O Go ($\overline{\text{IOGO}}$) signal triggers the HP-IB processor to output the data. When the data is on the bus the I/O processor reads the data and identifing the command.

This command (HP-IB Write Data command) indicates to the I/O processor that the computer has print data for the printer. This print data must be stored into the shared I/O RAM memory using the master/slave shared memory communication protocol (described in paragraph 3-2). The I/O processor builds a packet for the printer control processor identifying the command and the amount and location of data involved. This packet data is written into the I/O RAM.

When the I/O processor is ready to accept the data from the HP-IB processor, the I/O processor will enable the HP-IB processor IOGO signal. When the $\overline{\text{IOGO}}$ signal is enabled the HP-IB processor outputs the data onto the interface bus and the I/O processor performs a read operation to read the data. This data byte is to be transferred into the I/O RAM memory.

For the I/O processor to write to the I/O RAM memory the I/O processor enables $\overline{\text{MREQ}}$ and $\overline{\text{WR}}$. These signals inform the control circuitry that the I/O processor requires access to the I/O RAM memory. The control circuitry determines if the I/O RAM memory is available (is not being accessed by the printer control processor). Since the I/O RAM memory is shared by the printer control processor and the I/O processor, only one processor may access the memory at a time. If the printer control processor is using the I/O RAM memory, the I/O processor may be required to wait. If the I/O RAM memory is not

available the I/O control circuitry will generate WAIT signals which will hold off the I/O processor from accessing the I/O RAM memory until it becomes available. When the I/O RAM memory becomes available the WAIT signal is discontinued and the I/O processor is given access to the I/O RAM.

To allow the I/O processor access to the I/O RAM memory the I/O control circuitry will enable the Gate (GATE) signal and the Direction (DIR) signal to allow the I/O processor data to pass through the gate to the memory. The I/O control circuitry enables the Address Select (AS) line to the Address Multiplexer to allow the I/O processor address to address the memory.

Each byte is transferred from the HP-IB processor across the bus into I/O processor and then back onto the bus into I/O RAM. For each byte the I/O processor selects an I/O RAM address, outputs the address across the address bus to write the data into the memory.

The I/O processor addresses and places the data byte onto the bus. The I/O RAM memory will shift the bytes into its memory when Write Enable (WE) signal from the I/O control circuitry becomes active.

Each byte of data received by the HP-IB processor is transferred into memory in this manner until all the data is transferred. When the final data byte is received by the HP-IB processor, the HP-IB processor enables the EOSINT interrupt line. This indicates to the I/O processor that the data transfer is complete. Now the I/O processor will complete the packet information and write it into the packet memory location. When the data transfer operation is complete the I/O processor will interrupt the printer control processor to let it know that the interface shared I/O RAM contains information for the printer control processor.

The I/O processor interrupts the printer Control Processor by enabling the Interrupt Master (INTMAS) signal. Since any one of several slaves can enable the INTMAS signal line and the printer control processor cannot identify which slave has interrupted, the printer control processor will poll the slaves one at a time to identify the one requiring service. To identify the interrupting slave the printer control processor enables the Interrupt Acknowledge (INTACK) signal line. This line is common to all slave circuits. Any slave which interrupted the printer control processor will respond by enabling its Poll Acknowledge (POLACK) signal line. Each slave circuit has its own unique POLACK signal line which identifies to the printer control processor the source of the interrupt. When the printer control processor is ready to accept data from the interface, it will respond to the interrupt request by the interface.

For the printer control processor to communicate with the interface the printer control processor must access the I/O RAM and retrieve the information (packet and data) placed there by the I/O processor. For the printer processor to address the I/O RAM, it must gain access to the I/O ram in the same manner as the I/O processor. The printer control processor will enable its Memory Request (MEMREQ) and Read (RD) signals to the I/O control circuitry. If the I/O processor is not using the I/O RAM for any operation the I/O control circuitry will allow the printer control processor access to the I/O RAM. For the printer control processor to access the RAM the I/O control circuitry enables the bi-directional bus gate A allowing the printer control processor to access the I/O RAM across the bus. The control circuitry will also enable the I/O Address Multiplexer to allow the Address Select signal to the Address Multiplexer to pass the master address bus addresses to the I/O RAM.

Thus the data from the computer is passed through the HP-IB interface to the printer. The transfer of data from the printer to the computer through the interface is identical except the direction is reversed.

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SECTION IV. MAINTENANCE

4-1. INTRODUCTION

This section provides troubleshooting information and parts replacement information for the HP-IB interface.

4-2. SELF-TEST

The HP-IB interface contains a self-test diagnostic program which is checks the I/O ROM, I/O RAM, and and most of the HP-IB processor operations.

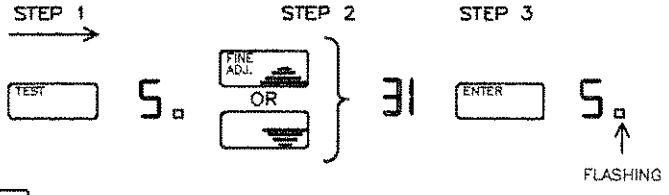
This self-test diagnostic is resident in the interface I/O RAM memory and is initiated from the printer Operator Control Panel by selecting subtest number 31. The standard printer test (self-test) does not perform the I/O subtest diagnostic (except when the printer is, in CE mode), the I/O subtest must be selected and ran separately

If the I/O self-test is initiated and completes satisfactorily the printer displays the printer-ready status (0 is displayed); if an error is detected the printer display flashes 50 to indicate an I/O error. To identify the type of error press the ENTER key and the I/O self-test error code number (refer to table 4-2) should appear in the display. If the printer is looping on the I/O subtest, then the panel displays a 4 (to indicate looping). If an error is detected while looping, looping stops and the I/O error number 50 will flash in the display.

The I/O subtest performs three routines which check the I/O RAM, I/O ROM, and HP-IB processor, if any one of these tests fail an error number (code) is displayed in the printer Operator Control Panel. Also, if any two or all three of the routines fail, a multiple-error number is provided. These error numbers for the subtest routines are listed in table 4-2 below.

To run the self-test diagnostic perform the following operations:

- To run the HP-IB I/O subtest:

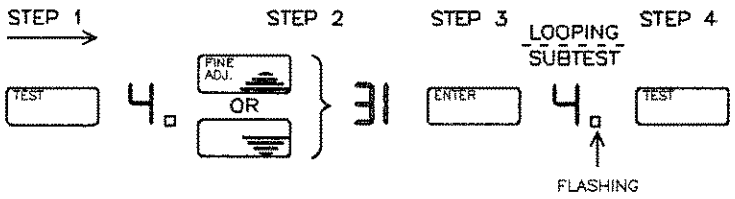


1 - Press the [TEST] key until a 4 appears in the Operator Control Panel display.

2 - Select the HP-IB I/O subtest number (31) in the printer Operator Control Panel display.

3 - Press the [ENTER] key to run the subtest.

- To run the HP-IB I/O subtest continuously (loop):



1 - Press the [TEST] key down until a 4 appears (a 5 will appear first then the 4; it takes approximately it five seconds for the 5 to appear), in the Operator Control Panel display.

2 - Select the HP-IB I/O subtest number (31) in the printer Operator Control Panel display.

3 - Press the [ENTER] key to run the subtest.

4 - Press the [TEST] key to terminate the continuous subtest (if an error is detected the testing will stop and a flashing 50 will appear in the Operator Control Panel display).

TABLE 4-1. I/O SELF TEST ERROR CODES

ERROR NUMBER	ERROR DESCRIPTION
00	NO ERRORS DETECTED
01	RAM ERROR
02	ROM ERROR
03	HP-IB PROCESSOR ERROR
04	MULTIPLE FAILURES

4-3. I/O LED

When the interface is powered-up or the printer is reset the interface performs the HP-IB I/O self-test and the I/O processor performs some initial communication with the printer processor. If the communications is performed satisfactorily and the HP-IB I/O self-test completes with no errors the service LED will flash at a 1 Hz rate. If the interface fails the subtests on power-up, the led will not flash, remaining either steady on or off. If the interface pases the I/O subtest but fails to complete the initial communication process the service LED will flash at an 5 Hz rate. If the service LED is flashing at the 5 Hz rate a malfunction in the I/O processor or the I/O control circuitry is indicated. This assumes that the printer processor circuits are capable of communicating with the interface. To eliminate the possibility of a printer circuit malfunction, the printer standard self-test should be performed first to ensure the operation of the printer circuits.

4-4. REPLACEMENT PARTS AND DIAGRAMS

The replacement parts, diagrams, and schematics are provided in tables and figures provided on the following pages.

TABLE 4-2. SERVICE LED ERROR INDICATIONS

LED	ERROR DESCRIPTION
1/2 Hz FLASH	Interface operating correctly.
5 Hz FLASH	Passed I/O self-test but failed to communicate with printer processor (I/O processor or printer control processor failure)
ON or OFF STEADY	Interface failed subtest (I/O RAM, ROM, or HP-IB processor failure likely). Also front panel cable, can cause this error.

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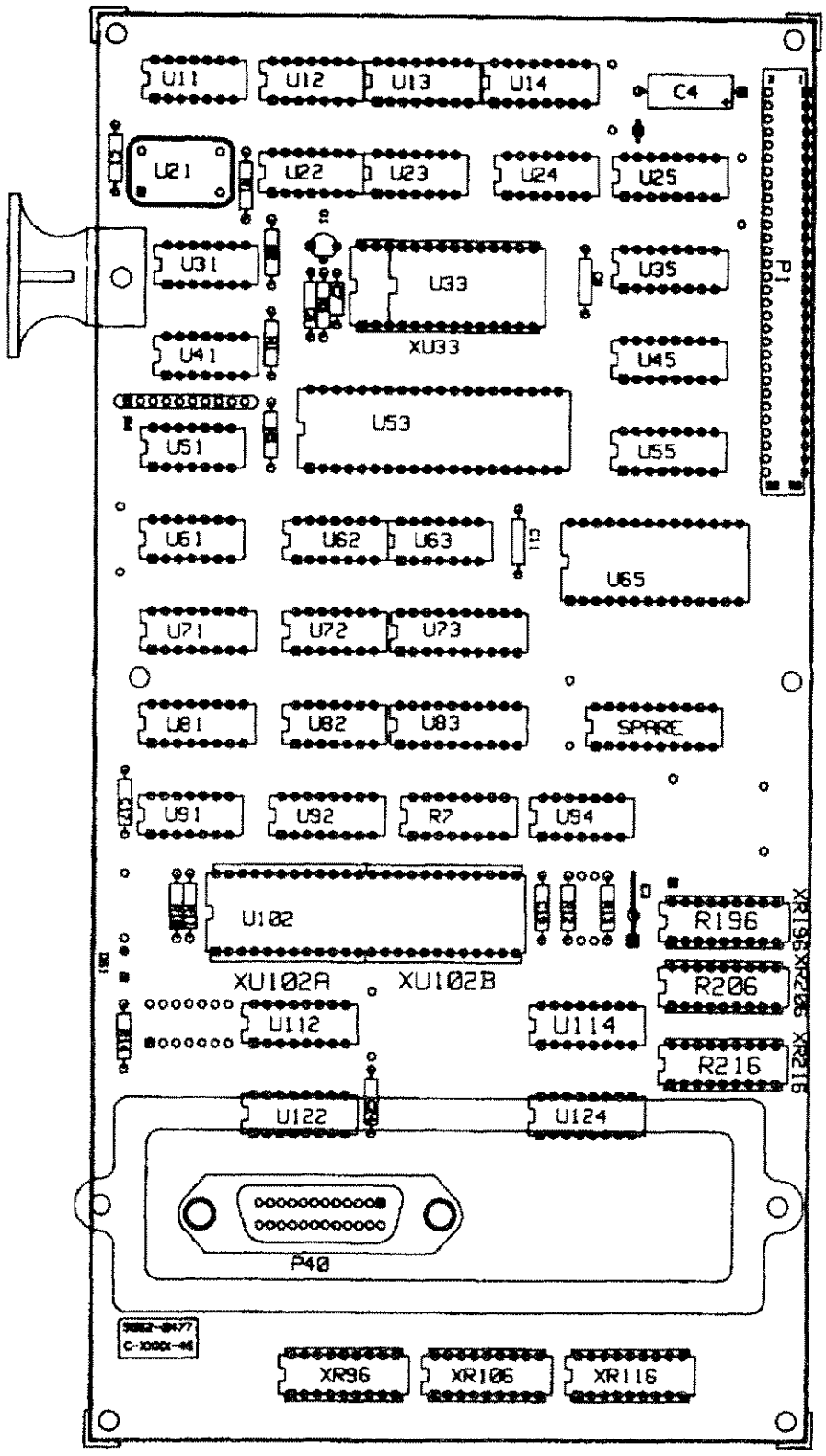


Figure 4-1. HP-IB Interface PCA (5062-0477) Parts Location

TABLE 4-3. HP-IB INTERFACE PCA (5062-0477) PARTS LIST

REF. DES./ INDEX NO.	DESCRIPTION
C7	C:F 33PF 5% 100V
C1,6,8,11, C17,19,24	CAP: .01UF 10% 100V
C4	C:F 22UF 25V AL
6	STDF:RVT #6X.188
8	STDOFF:HEX M/FM
2	EXTR PC BD
3	RSCR-MCH M3X8 LG
4	NUT: HEX
R10,11,13, R14	R:F 2.15K 1%.125
R1,2,5	R:F 21.5 1% .125W
R3	R:F 34.8K 1% .125
R12	R:F 21.5K 1% .125
XR96,106,116, 196,296,216	SOCKET:18 PIN IC
XU102A,XU102B	SCKT: 24 PIN IC
XU33	SCKT: 28 PIN IC
P40	CONN: 24 PIN F
E3	TAB-MALE PC
P1	SCKT: 28 PIN IC
R4	N:R9X2.2K 2% .125W
R196	N:R 16X3K/6.2K
R216	N:R 16X750/1.5K
R206	N:R 16X1.5K/3.1K
R7	NET-RES:4.7KX15
U21	OSC: XTAL CK
U65	IC HM6264LP-15
U33	ROM: HPIB FW 2338
U82	IC: SN74S03N GATE
U11,31,51,61	IC: 74S74N
U12	IC: SN74LS02N
U24,72	IC: SN74LS00N
U63	IC: SN74LS51N
U22,62	IC: SN74LS51N
U13,14	IC: SN74LS279N
U35,45,55	IC: SN74LS298N
U92	IC: SN74LS368AN
U41	IC: SN74LS126AN
U112,114,122, 124	IC: MC3448AL
U53	IC: Z80A-CPU-PS
U94	IC: SN74ALS74N
U23	IC: SN74ALS32N
U91	IC: SN74ALS10N
U25,81	IC: SN74ALS138N
U71	IC: SN74ALS175N
U73,83	IC: SN74ALS645AN
Q1	XSTR: PNP 2N3906
U102	MEDUSA-CHIP
9	WSHR: #10SPL LOCK
W1	WIRE: 22AWG JMP
5	LBL: IMPRINTABLE
7	PLATE: 24P RIBBON
1	PCB: HPIB I/O

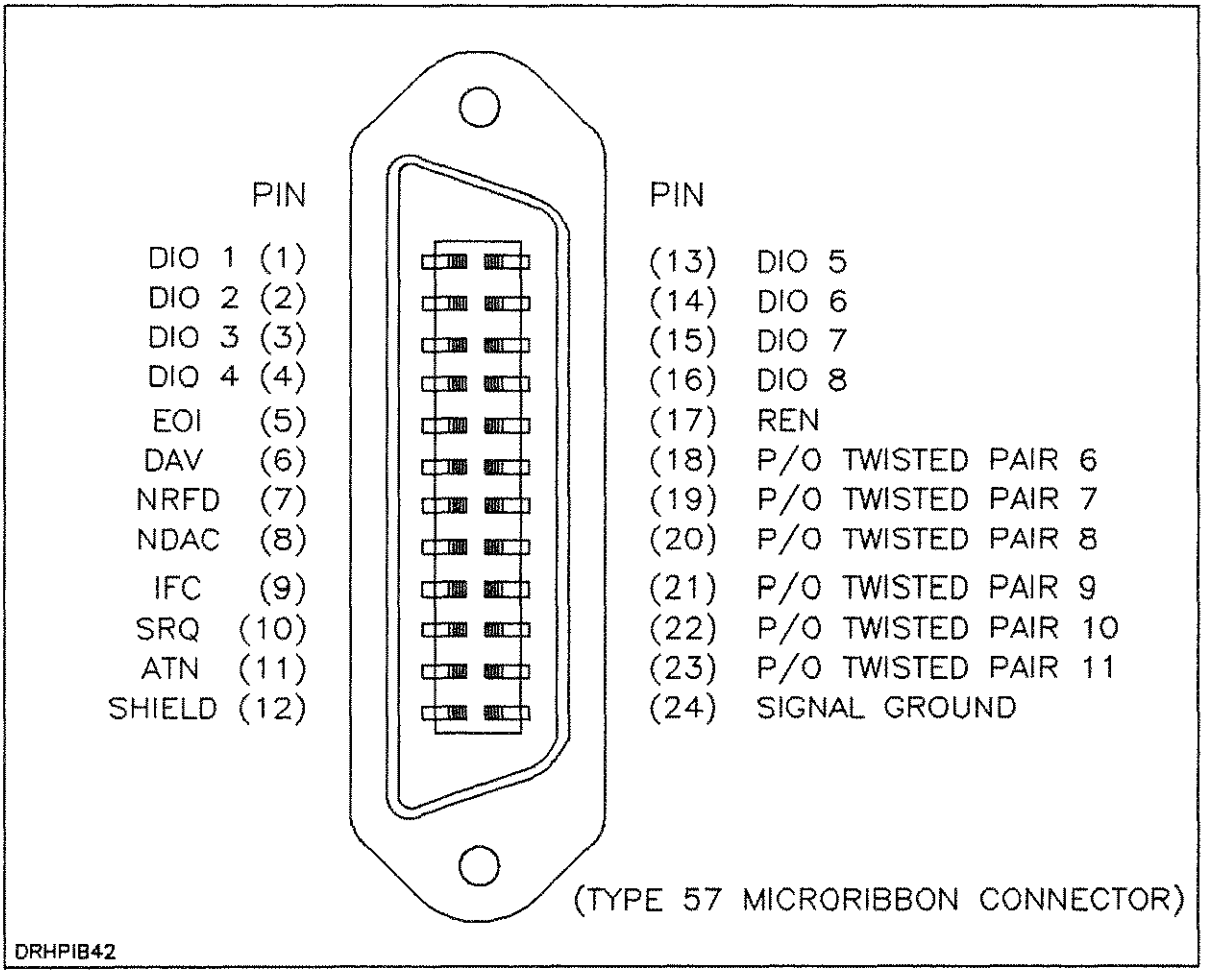


Figure 4-2. HP-IB Connector (P40) Signal Connections

TABLE 4-4. INTERFACE BACKPLANE CONNECTOR (P1) SIGNAL CONNECTIONS

PIN	SIGNAL	PIN	SIGNAL
1	+5	2	+5
3	+5	4	+5
5	Reserved	6	VSERVO
7	+12	8	+12
9	-12	10	-12
11	GND	12	GND
13	GND	14	GND
15	SCLOCK	16	SPASE
17	/FIRE	18	/NMI
19	/HMRDATA	20	/SPASE
21	/IOREQ	22	/MEMREQS
23	/RESET	24	/INTMAS
25	[CLOCK 7 to 8 MHz]	26	/WAIT
27	/RD	28	/WR
29	A0	30	A1
31	A2	32	A3
33	A4	34	A5
35	A6	36	A7
37	A8	38	A9
39	A10	40	A11
41	A12	42	A13
43	A14	44	A15
45	S0	46	S1
47	S2	48	S3
49	D0	50	D1
51	D2	52	D3
53	D4	54	D5
55	D6	56	D7
57	/INTACK	58	/POLACK
59	/IOREQ	60	/MEMREQ

"/" Indicates the signal is NOTed.

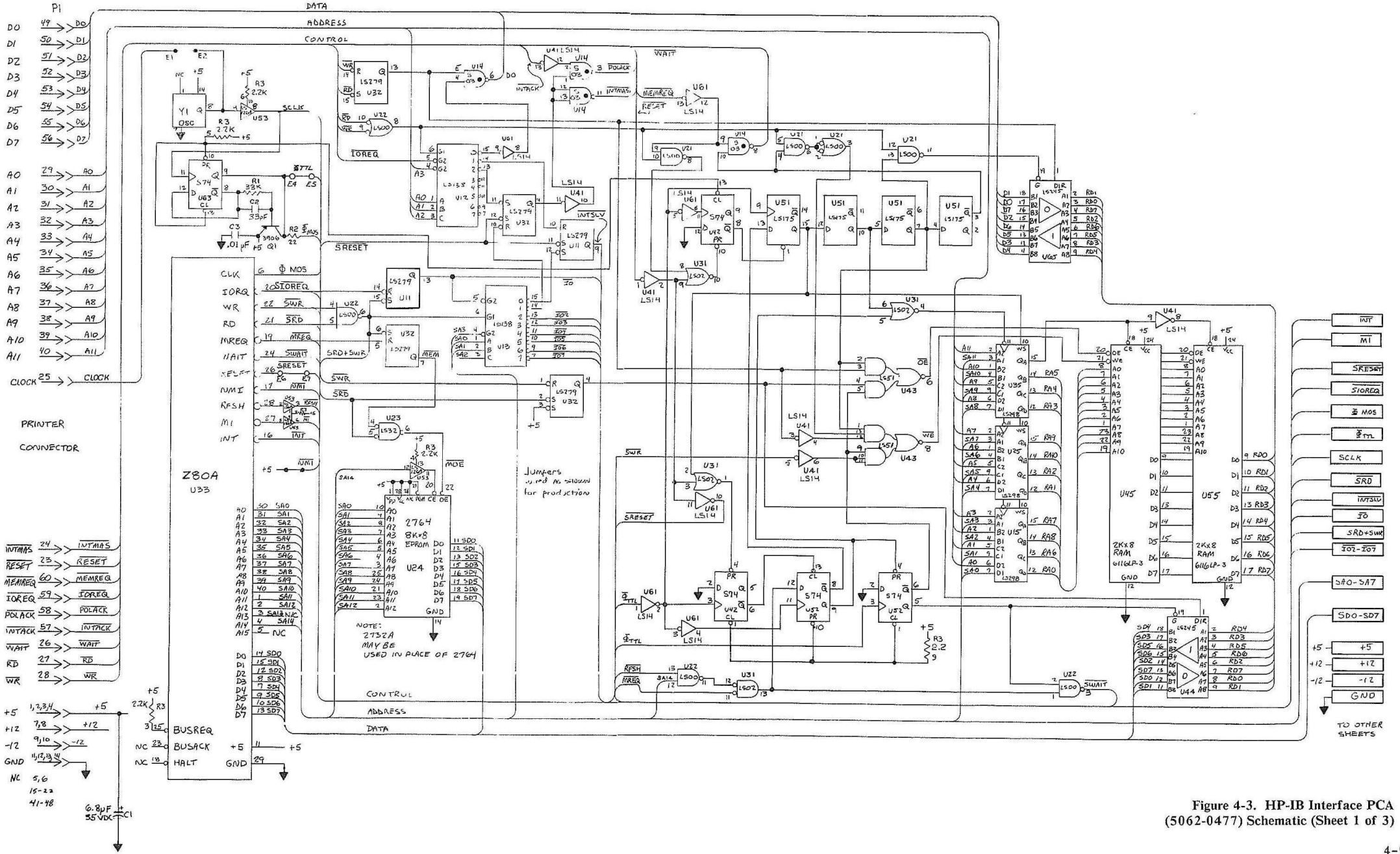


Figure 4-3. HP-IB Interface PCA (5062-0477) Schematic (Sheet 1 of 3)

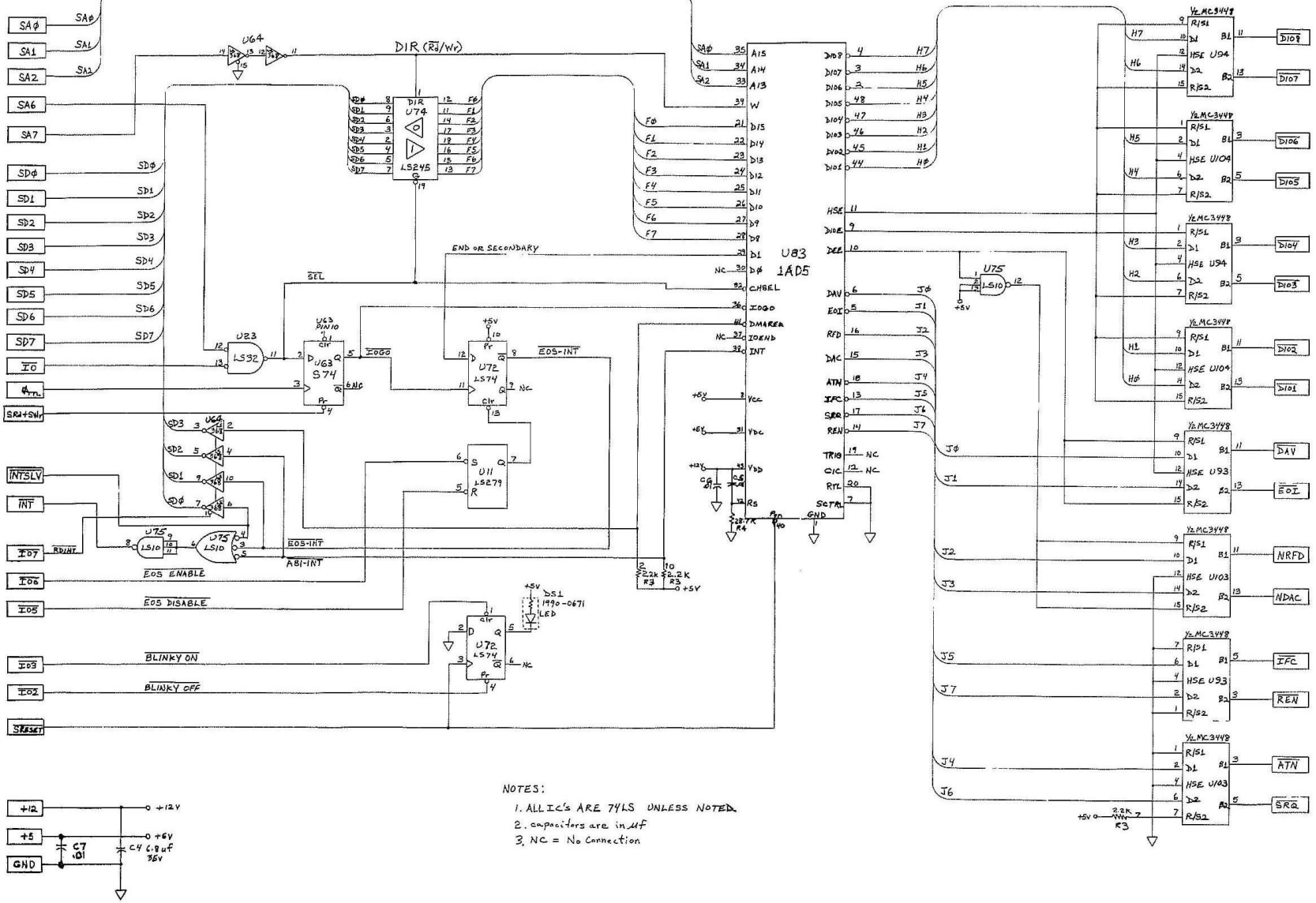
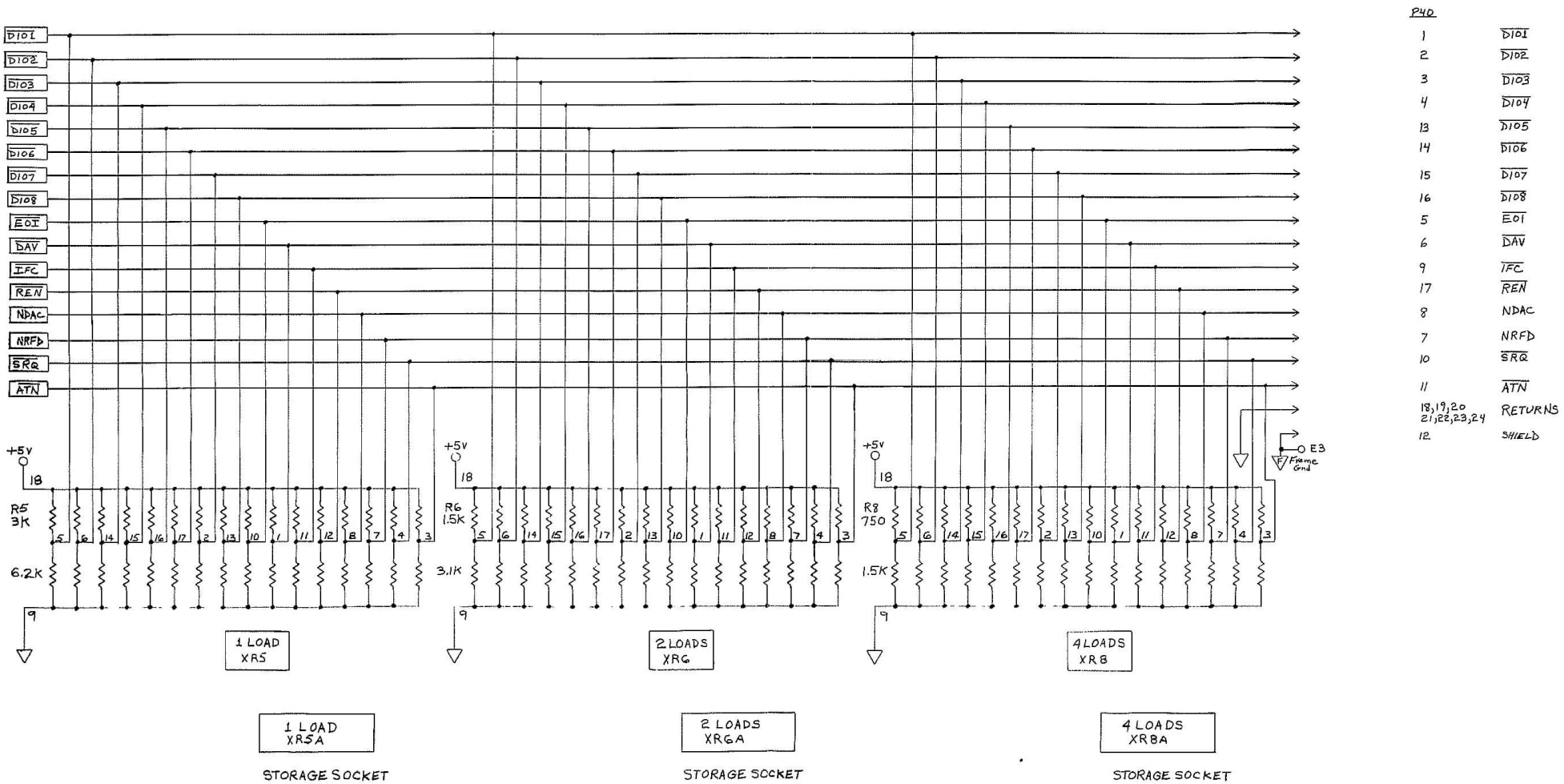


Figure 4-3. HP-IB Interface PCA (5062-0477) Schematic (Sheet 2 of 3)



P4D	
1	DIO1
2	DIO2
3	DIO3
4	DIO4
13	DIO5
14	DIO6
15	DIO7
16	DIO8
5	EOI
6	DAV
9	IFC
17	REN
8	NDAC
7	NRFD
10	SRQ
11	ATN
18,19,20 21,22,23,24	RETURNS
12	SHIELD

Figure 4-3. HP-IB Interface PCA (5062-0477) Schematic (Sheet 3 of 3)

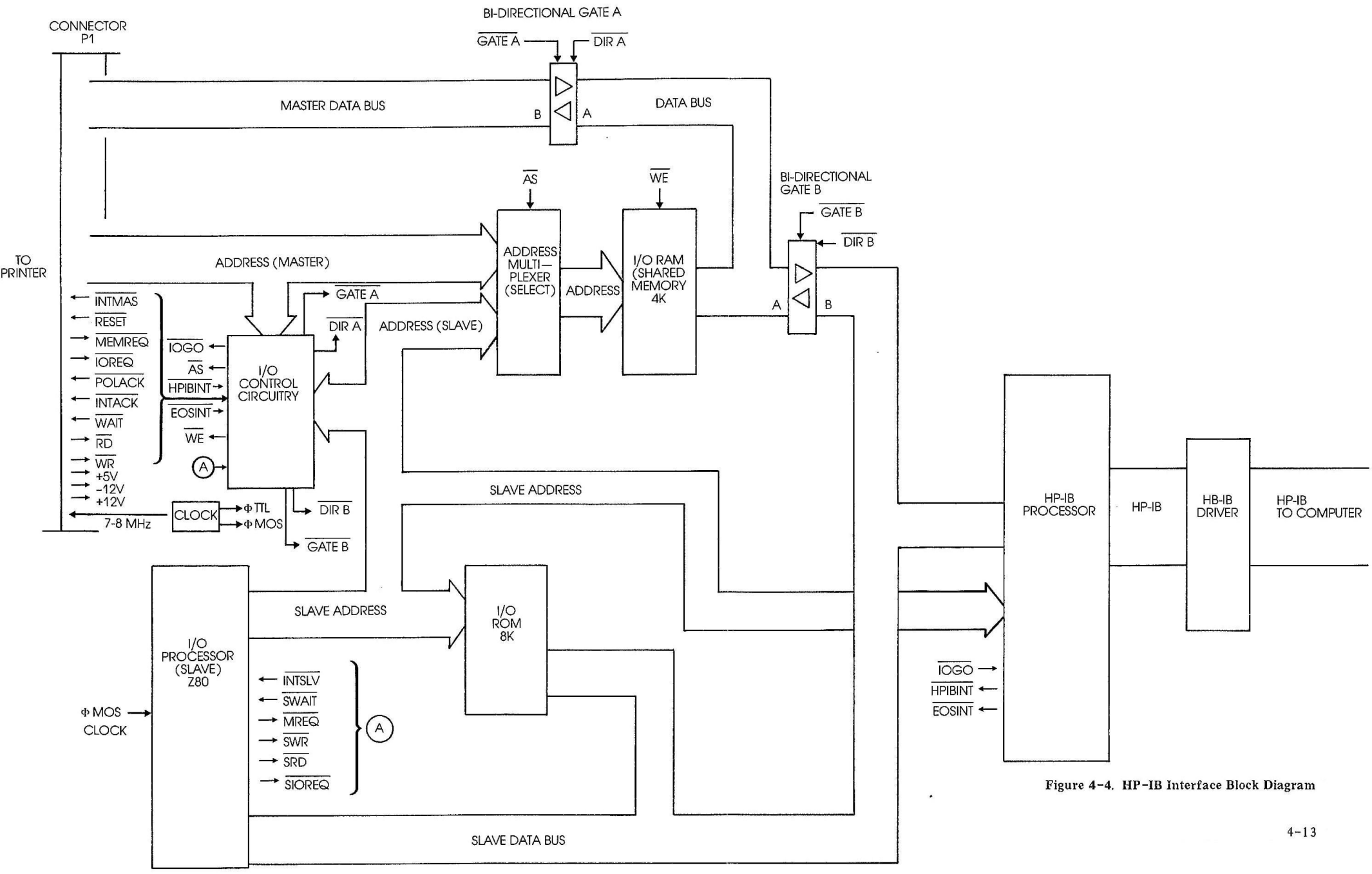


Figure 4-4. HP-IB Interface Block Diagram