HP 3000
HARDWARE
ARCHITECTURE

BLOCK DIAGRAM
DIRECT I/O
START I/O

CHANNEL PROGRAMMING
SIO MULTIPLEXER
PORT CONTROLLER–
SELECTOR CHANNEL

DIRECT I/O

The ability of the computer to communicate with an I/O device on a one word per instruction basis.

START I/O

The ability of the computer to set up multi–word transfers between memory and I/O devices.

CHANNEL PROGRAMMING

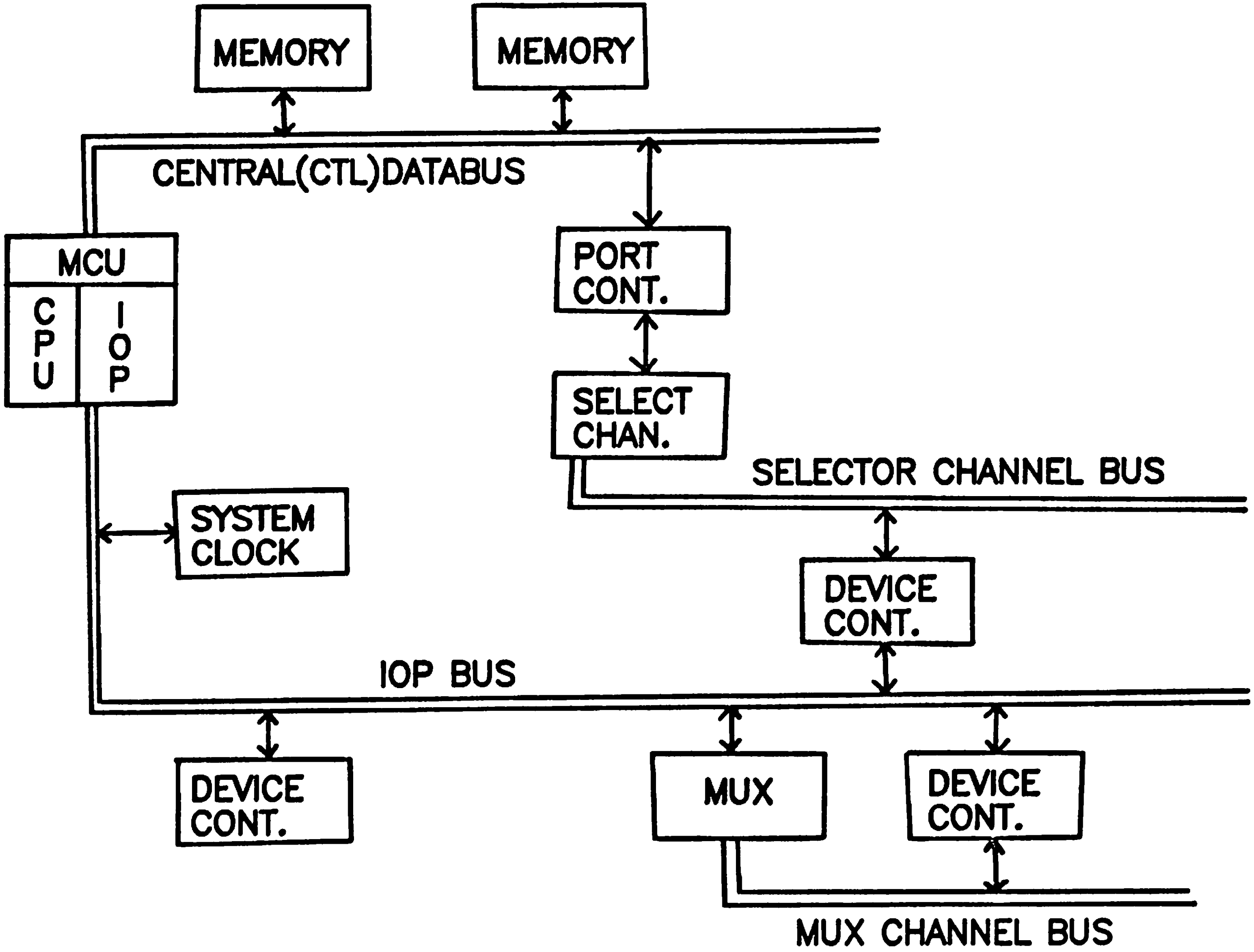
The program instructions used to control the transfers in the start I/O mode.

SIO MULTIPLEXER

The hardware subsystem that controls the execution of the channel programs on up to 16 I/O devices at a time.

PORT CONTROLLER–SELECTOR CHANNEL

The hardware subsystem that controls the execution of the channel programs on high speed devices.



MEMORY

MEMORY

CENTRAL(CTL)DATABUS

MCU

CPU

IOP

PORT CONT.

SELECT CHAN.

SELECTOR CHANNEL BUS

SYSTEM CLOCK

DEVICE CONT.

IOP BUS

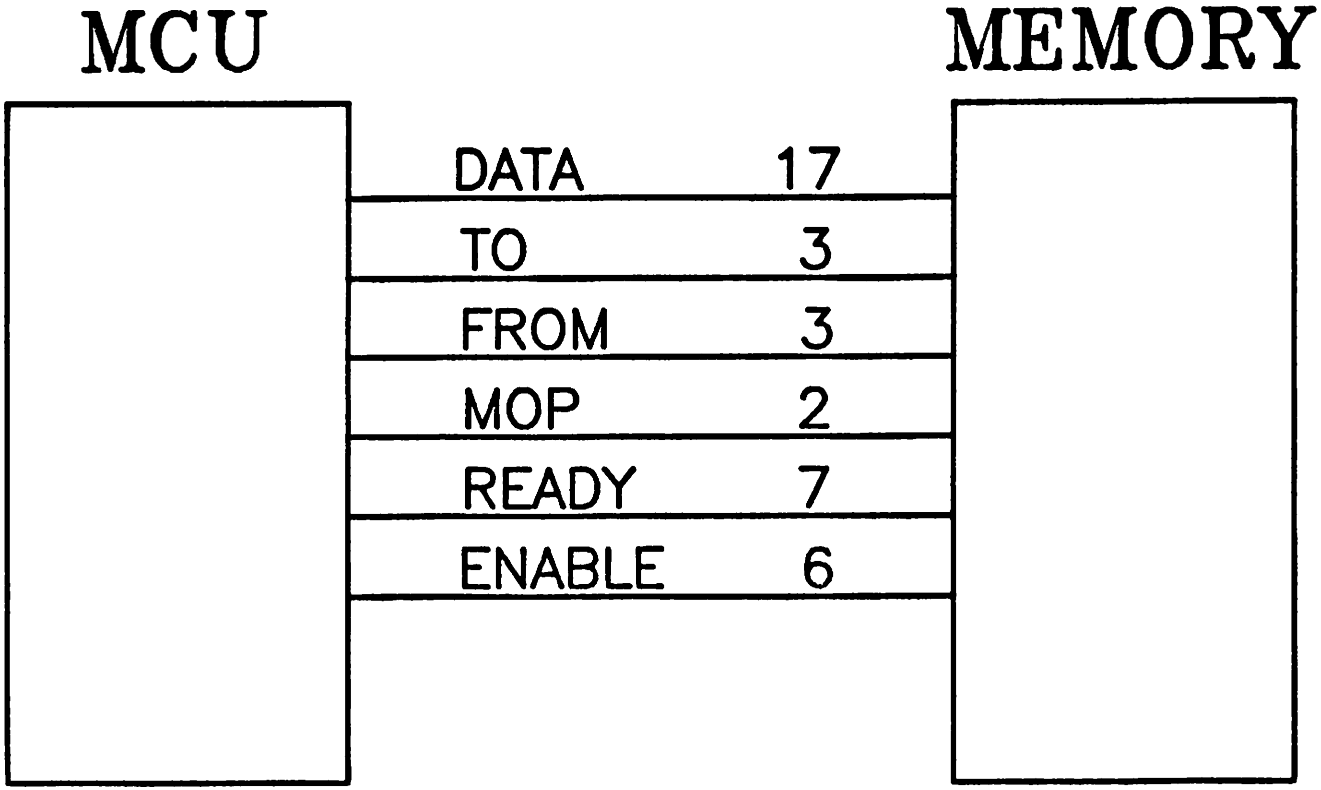
DEVICE CONT.

MUX

DEVICE CONT.

MUX CHANNEL BUS

CTL BUS

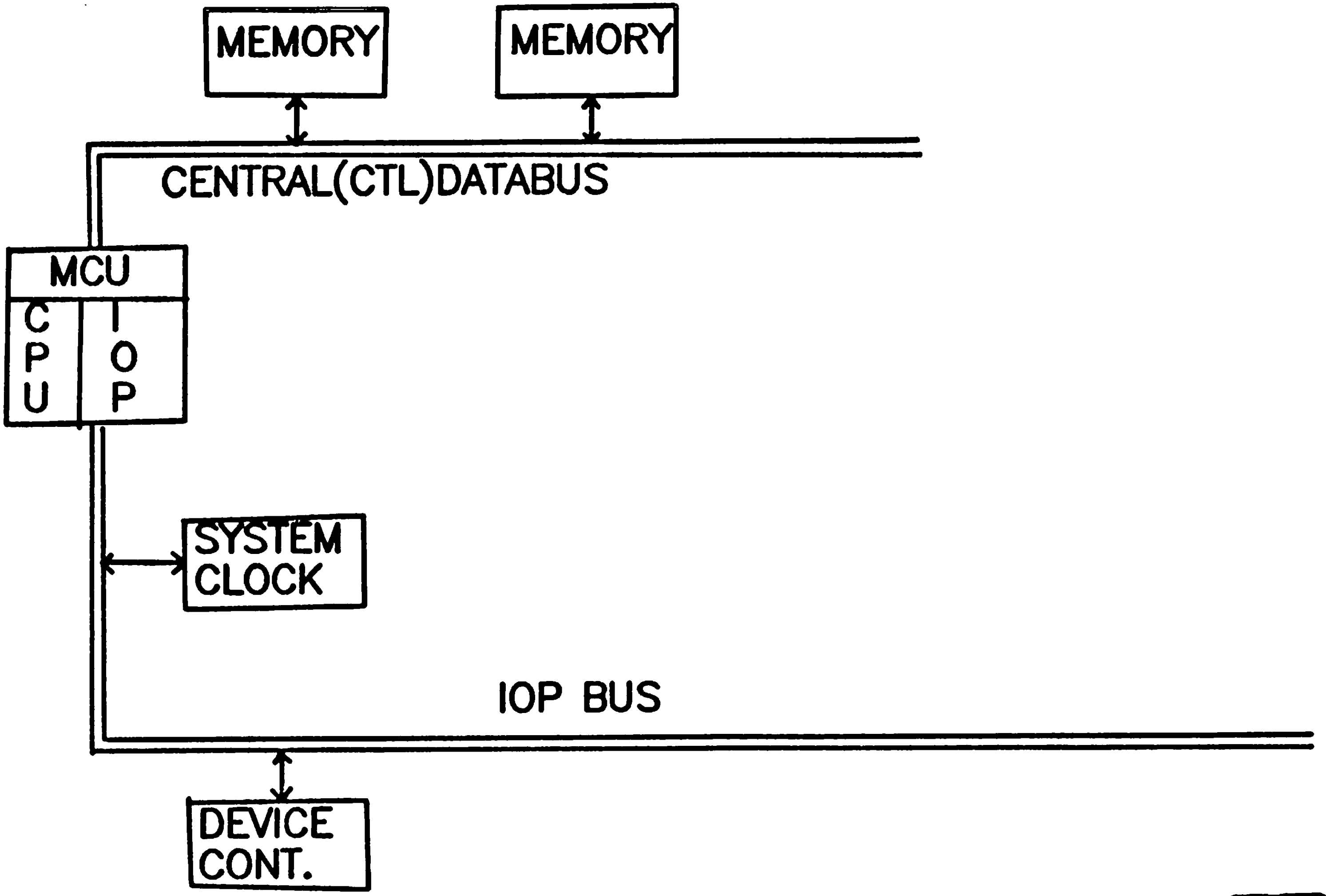


MCU

MEMORY

DATA	17
TO	3
FROM	3
MOP	2
READY	7
ENABLE	6

DIRECT I/O


MEMORY
MEMORY
CENTRAL(CTL)DATABUS
MCU
CPU
IOP
SYSTEM CLOCK
IOP BUS
DEVICE CONT.

DEVICE CONTROLLER

The hardware that interfaces the iop bus to an I/O device.

IOP

The hardware that interfaces the cpu to the iop bus.

DRT NUMBER

A number to which only one DC will respond.

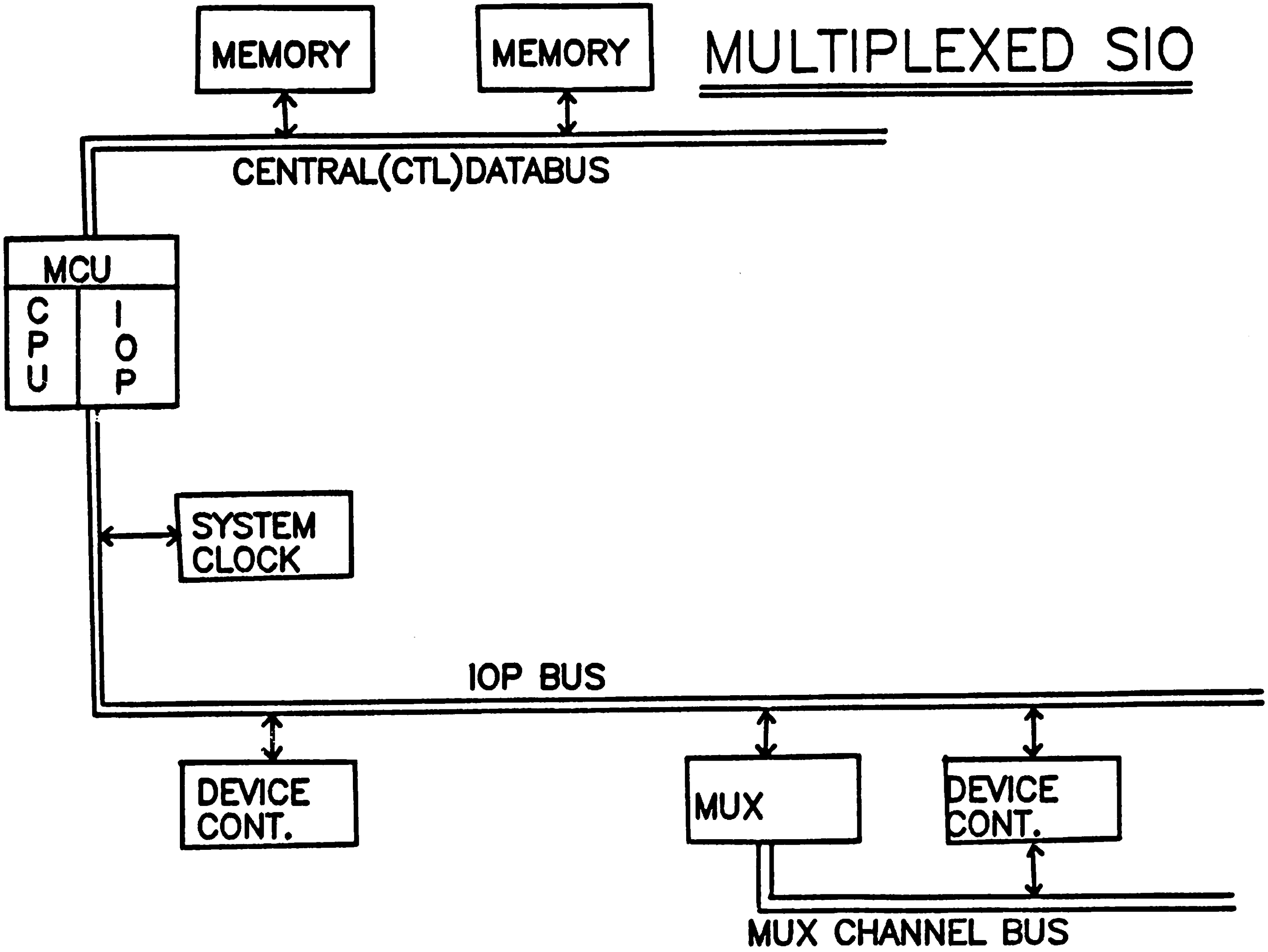
IOP BUS

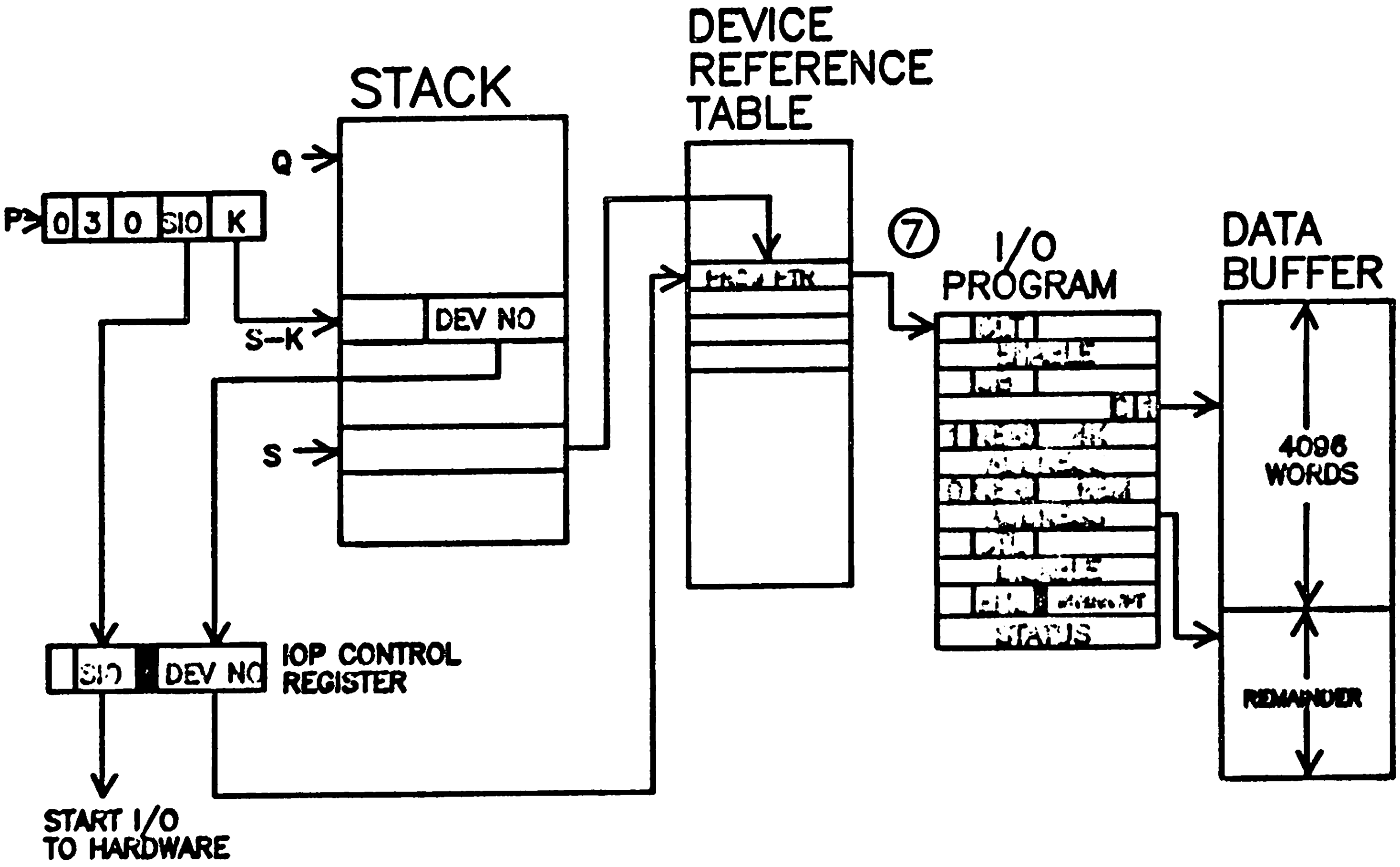
A multi lined cable which connects the iop to all device controllers. It carries data, drt number and handsake signals

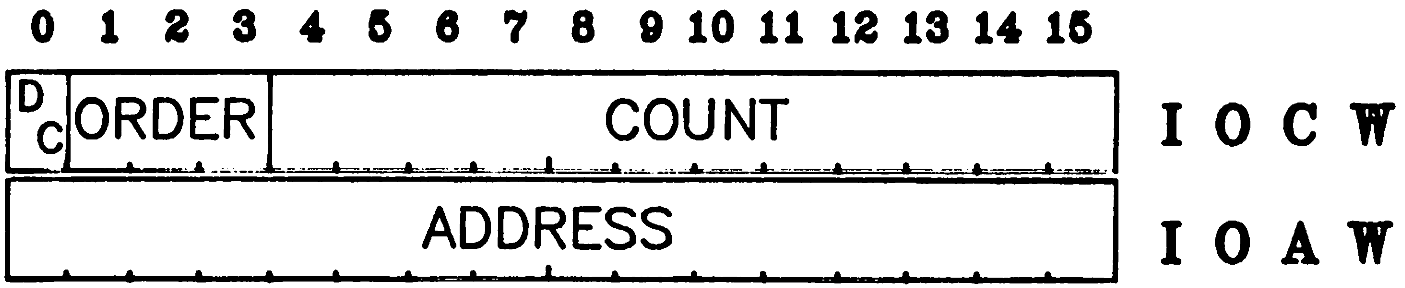
COLD LOAD ON DRT 6

```
30   000031   PROG POINTER
31   014000   SET BANK
32   000000   BANK NUMBER
33   040000   CONTROL
34   000006   CONTROL WORD (READ)
35   077740   READ 32 WORDS
36   000037   READ TARGET ADDRESS
37   034000   END-JUST IN CASE
```

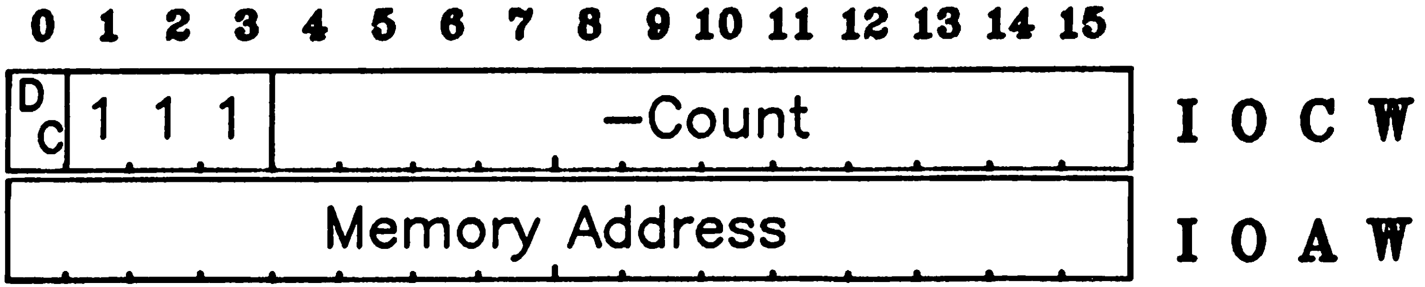
MULTIPLEXED SIO




STACK
DEVICE
REFERENCE
TABLE
Q
P
0
3
0
SIO
K
S–K
DEV NO
S
⑦
I/O
PROGRAM
1
0
STATUS
DATA
BUFFER
4096
WORDS
REMAINDER
SIO
DEV NO
IOP CONTROL
REGISTER
START I/O
TO HARDWARE


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
DC
ORDER
COUNT
I O C W
ADDRESS
I O A W

READ



0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

DC 1 1 1 −Count IOCW

Memory Address IOAW

WRITE

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
D C	1	1	0	−Count												I O C W
Memory Address																I O A W

CONTROL

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	1	0	0	I/O Command Code 1												IOCW
I/O Command Code 2																IOAW

END

If Bit 4 Then Interrupt

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	1	Not Used											IOCW
Returned Device Status																IOAW

SENSE

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	1	0	1	Not Used												IOCW
Returned Device Status																IOAW

INTERRUPT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	0	Not Used												I O C W
Not Used																I O A W

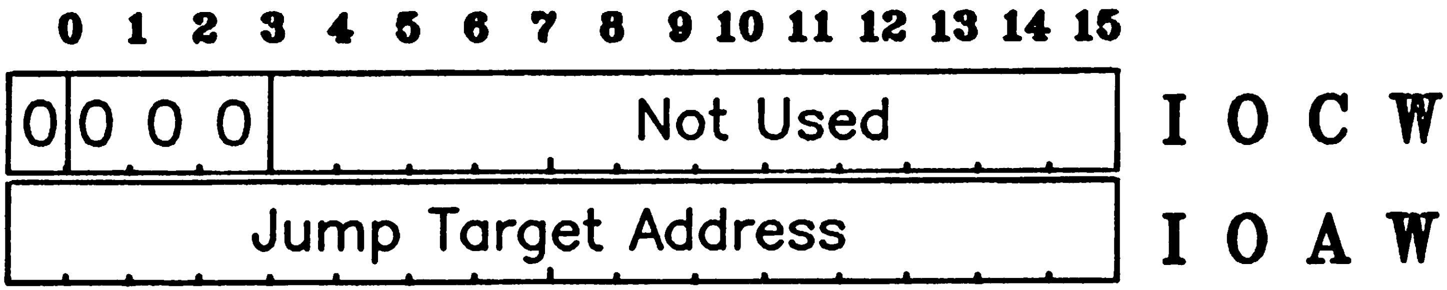
SET BANK

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	0	1	1	Not Used											I O C W
Not Used												Bank #				I O A W

RETURN RESIDUE

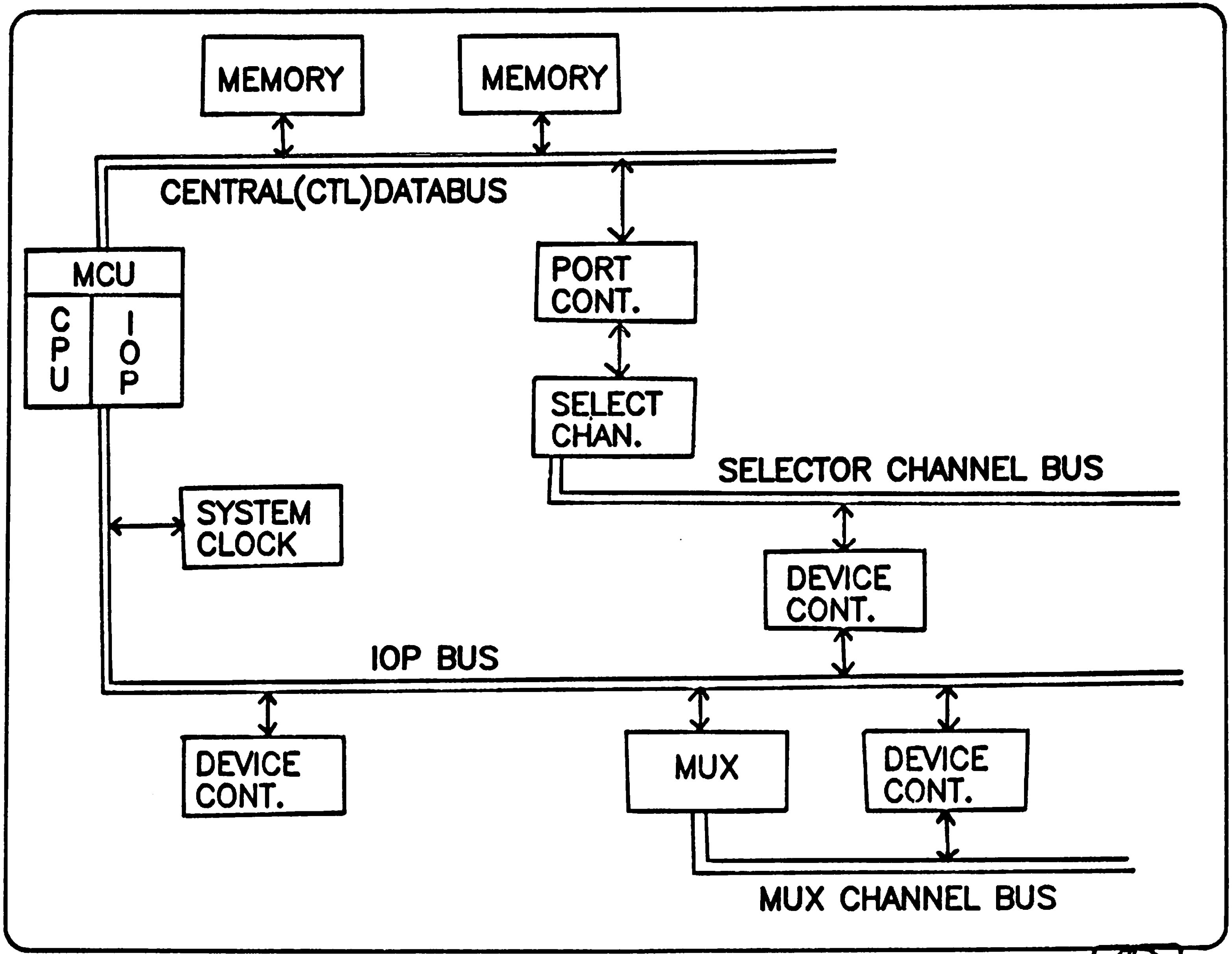
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	0	1	0	Not Used											I O C W
Returned Count (Residue)																I O A W

JUMP


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 0 0 0 Not Used
I O C W
Jump Target Address
I O A W

COLD LOAD ON DRT 6

30	000031	Prog Pointer
31	014000	Set Bank
32	000000	Bank number
33	040000	Control
34	000006	Control word(read)
35	077740	Read 32 words
36	000037	Reads target address
37	034000	End–Just in case



MEMORY

MEMORY

CENTRAL(CTL)DATABUS

MCU

CPU

IOP

PORT CONT.

SELECT CHAN.

SELECTOR CHANNEL BUS

SYSTEM CLOCK

DEVICE CONT.

IOP BUS

DEVICE CONT.

MUX

DEVICE CONT.

MUX CHANNEL BUS

DRT FETCH

Mux. tells the IOP. to read memory

Mux. tells the DC to give its device # times 4 as the address to be read

IOP reads memory and puts the returned word on the IOP BUS. It then updates the word by 2 and writes it back

Mux stores this word and advances to the next state "IOCW FETCH"

IOCW FETCH

Mux. tells the IOP to do a read and gives the word it just recieved as the address to be read

IOP reads memory and puts the returned word on the IOP BUS

Mux. stores this word and advances to the next state "IOAW FETCH"

IOAW FETCH

Mux. tells the IOP to do a read and gives the (word read in the DRT FETCH STATE)+1 as the address to be read

IOP reads memory and puts the returned word on the IOP BUS.

Mux. stores this word and advances to the next state.

DATA read

Mux. tells the IOP to do a write and gives its address register as the address to be written

Mux. tells the DC to give its data register as the word to be written

IOP writes the data into the given address

Mux. updates the address register by 1 and counts the word count by 1

If the word count rolls over then advance
to the next state "DRT FETCH"
else same state

DATA write

Mux. tells the IOP to do a read and gives its address register as the address to be read

IOP reads memory and puts the returned word on the IOP BUS

Mux. tells the DC to store this word into its Data register

Mux. updates the address register by 1 and counts the word count by 1

If the word count rolls over then advance to the next state "DRT FETCH" else same state